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HIGH SPEED PROBABILISTIC ADDER FOR SIGNAL PROCESSING SUBSYSTEMS

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ABSTRACT

This study proposes a new high performance and low power adder using new design style called probabilistic is proposed. The design of a probabilistic adder that achieves low power and high speed operation. The delay and power dissipation are reduced by dividing the adder into two parts to reduce the carry chain. This dividing approach reduces active power by minimizing extraneous glitches and transitions. It is an approach for the design and comparison of 16-bit adders for low-power signal processing applications. Simulation and Synthesis results show that the proposed adder outperforms the conventional adders in terms of power consumption, delay and transistor count.

Keywords: Power Delay Product, Signal Processing, Low Power Design, Probabilistic Approach, Acceptable Accuracy

1. INTRODUCTION

Addition is a fundamental arithmetic operation that is broadly used in many communication systems, DSP architectures and microprocessors. The design of adder having low power consumption and low propagation delay results of great interest for the implementation of modern digital systems. As a result, several adder designs, such as carry ripple adder, carry select adder, carry look-ahead, conditional sum adder, carry skip adder and various prefix adders are available to satisfy various area, delay and power requirements. The carry select adder (Ramkumar and Kittur, 2012) has less area because it uses different pair of RCA to produce fractional sum and carry output. In this gate level modification of square root carry select adder has high delay and PDP for smaller input operand additon process. The ripple carry and Manchester carry chain adders are the simplest, but slowest adders with O (n) area and O (n) delay, where n is the operand size in bits. Carry look-ahead, conditional sum and parallel prefix adders have O (n log (n)) area and O (log (n)) delay, but typically suffer from irregular layout. Carry-Skip-Adder (CSK) was initially proposed to improve the speed of a Ripple-Carry-Adder (RCA) with only a minimal overhead in number of gates. In Carry Save Adder (CSA), each block is processed conditionally. The carry in block is conditionally selects the carry out and sum-bits of the block (Weste and Eshraghain, 2010).

The critical path of CSA is either the ripple- carry path in the largest block or the worst case carry- select path. The optimal block sizing is chosen such that the delay of the ripple and carry select paths are balanced. A new test pattern is generated for detecting the acceptable error to increase the yield. The output masking is only applicable for detecting the smaller number of acceptable error (Hsieh *et al*., 2007). The concept of error tolerance (Shin and Gupta, 2011) and the PCMOS technology are important in signal processing systems. Any circuit is error tolerant if: (1) it contains defects that cause internal and may cause external errors and (2) the system that incorporates this circuit produces an acceptable outputs. This defect condition is not considerable one. The error-tolerant

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circuit was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS, 2003). Of course, not all digital systems can engage the error tolerant circuit. A system level error tolerance approach is used to estimate the acceptable error (Chong and Ortega, 2005) in harware part of the multimedia system. The error rate threshold and quantization noise of this system level techniques are depends on the acceptable degration. The error rate base test method is to increase the yield of some system with acceptable error (Lee *et al*., 2005). In this error tolerance based testing method is to compare the estimated fault with acceptable fault of the chips.

The digital control systems, the exactness of output signal is important and this avoids the use of error tolerant circuit. Many Digital Signal Processing (DSP) systems that process signals relating to human senses, the image processes and speech processing systems, the error-tolerant circuit is used (Zhu *et al*., 2010). In Error Tolerant Adder (ETA-I) contain an N-bit adder, it is divided into M (M≥2) blocks. Each block contains N/M bits and is consists of two separate circuitries -Sum and Carry generator. The Carry generator creates the carry output. It does not take the carry signal from previous block. The Sum generator is take the carry in signal from previous block to generate its sum output. The carry propagation only exists between two neigh boring blocks instead of lying along the entire adder structure. In design of ETAI, the dividing strategy refers to the choice of the number of blocks the adder is divided into fewer block. Some blocks are occupied and therefore extra bits are contained in single block. The possibility of receiving accurate outcome becomes higher while the delay path also becomes longer; on the contrary, if the adder is divided in a "better" approach, specifically extra blocks are occupied, the rate performance can be increased while the possibility that incorrect results can occur becomes higher.

The Error Tolerant Adder (ETA -II) occupies larger area (transistor counts) than conventional adders (Kim *et al*., 2011). However, there are always trade-offs between speed and power. The probabilistic design can be a potential solution to this problem. By sacrificing some accuracy, the probabilistic adder can attain great improvement in both the power consumption and speed performance. In this study contain an overview of the 16 bit adder design and then show how to extend the adder to quickly perform addition, which is useful in a variety of digital signal processing and multimedia applications.

The end around inverted carry adder (Vergos, 2012) is used to eliminate the race around condition occurred due to carry feedback. In this end around carry inverted adder occupies large area and also consumes high power as compared with other modulo adder.

In section 2, present the material and methods for proposed adder. In section 3, to show the results of proposed probabilistic adders with conventional adders. In section 4 is to disscus the power and transistor counts of an adder. In section 5 is to give the conclusions.

1.1. Probabilistic Addition

The first step is to divide the probabilistic adder into two parts in a definite method. The separating advance is based on an estimate and verify trick, depending on the necessities, such as precision, power and speed. Primary think about the delay of the proposed adder as Dp = max (Dd, Dp) where Dd is the delay in the deterministic part and Dp is the delay in the probabilistic part. With the suitable separating approach, on the way to make Dd roughly equal to Dp and hence achieve a best instance delay. With this separating approach scheme defined, then test whether the accuracy performance of the adder meets the requirements specified by the design engineer. For several applications, the necessity of the minimum acceptable accuracy should be 95% and the acceptance probability to be 98%. The proposed partition method must therefore have at least 98% of all possible inputs reaching an accuracy of better than 95%. If this necessity is not met, one bit must be shifted from probabilistic part to the deterministic part and have the checking process repeated. Due to the simplicity in structure and the removal of switching actions in the probabilistic part, putting more bits in this part yields more power reduction.

The probabilistic addition process, where the input operand is split into two parts: With higher order bits grouped into deterministic part and remaining lower order bits into probabilistic part. The length of each part need not necessary be equal. The addition process starts from the mid point toward the two opposite directions concurrently. The pattern of **Fig. 1**, two sixteen bit input operands, Ai = "1001101110110111" (40,053) and Bi = "1010111101101010" (45,116), are divided equally into 8 bits each for the deterministic and probabilistic parts. The addition of the higher order bits (deterministic part) of the input operands is performed from right to left (LSB to MSB) starting from the midpoint line with normal addition method is applied.

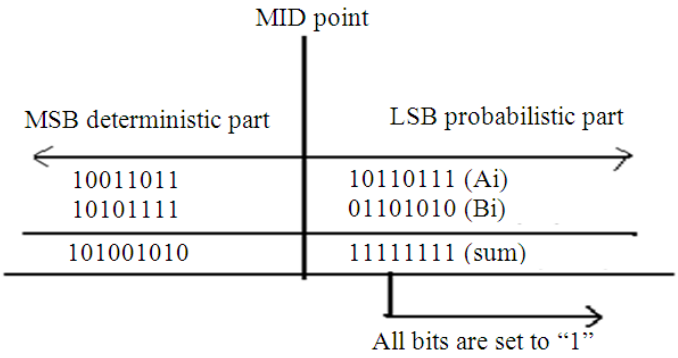

Fig. 1. Proposed addition process

To preserve its correctness since the higher order bits play a more important role than the lower order bits. The lower order bits of input operands (probabilistic part) are added using proposed addition process.

No carry signal will be generated or taken in at any bit position to eliminate the carry transmission pathway In the direction of reduce the overall inaccuracy owing in the direction of the elimination of the carry chain, check every bit position from left to right (MSB-LSB) starting from right of midpoint line; (1) if both input bits are "0" or dissimilar, the regular single bit adding is performed and the operation proceeds to next bit position; (2) the checking process is stopped when both input bits are encounter at the same time as high i.e., 1 and from this bit onwards, all sum bits to the right (LSB) are set to "1."

The addition process described can be easily understood from the example given in **Fig. 1** with a final result of "10100101011111111" (85,145) which should actually yield "10100101100100001" (85169) if normal arithmetic has been useful. In general inaccuracy can be computed as OE = 85,169-85,145 = 24. The accuracy of adder with respect to these two input operands is ACC = (1- (24/85169))×100 = 99.97%. This accuracy level is acceptable for most of the image and signal processing application. Consequently with eliminate carry transmission path in the probabilistic part and performing addition in two separate parts concurrently, on the whole a power consumption and delay time is greatly reduced.

1.2. Design of Probabilistic Adder

The probabilistic part consist of 8 bits and it is the most essential section in the proposed adder as it determines the accuracy, speed performance and power consumption of the adder. This probabilistic part consists of two blocks: The Control Signal Producing Block (CSPB) and the probabilistic addition block. The probabilistic addition block is made up of 8 advanced XOR gatesand each of which is used to generate a sum bit. The single block of advanced XOR gate is shown in **Fig. 2**. The Control signal producing block (Cspb) is consist of 8 Control Signal Producing Cells (CSPC) and each cell generates a control signal for the control input of probabilistic addition block.

The Control Signal Producing Block (CSPB) for 8-bit probabilistic part is shown in **Fig. 3**. Two types of control Signal Producing Cell (CSPC), labelled as type I and II are considered and the diagram implementations of these two types of CSPC are provided in **Fig. 4**. In this Control Signal Producing Cell (CSPC) is designed by both NOR and NAND gate. This design is compare over the conventional design to reduce the area. The Control Signal Producing Block (CSPB) is divided into two equally sized block for avoiding the propagation delay of the signal from the first cell to the last cell. CSPC-I is used within the CSPB and the CSPC-II is used for link between first CSPB to next CSPB.

Here the advanced XOR gate is designed by using the CMOS logic structure is shown in **Fig. 5a**. It consists of three inputs namely Ai, Bi, Control input (Ci) and single sum output. The control signal from the Control Signal Producing Cell (Cspc) is zero (Ci = 0), then the advanced XOR gate circuit is to operate in normal XOR gate. If the control signal is one (Ci = 1), then the advanced XOR gate output is set to (high) "1". When Ci is zero produced from CSPC is given in to the advanced XOR gate.

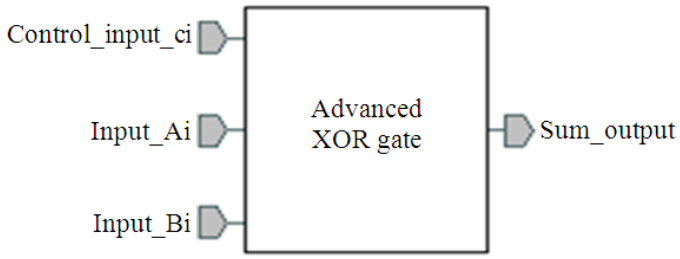

Fig. 2. Single block of advanced XOR gate

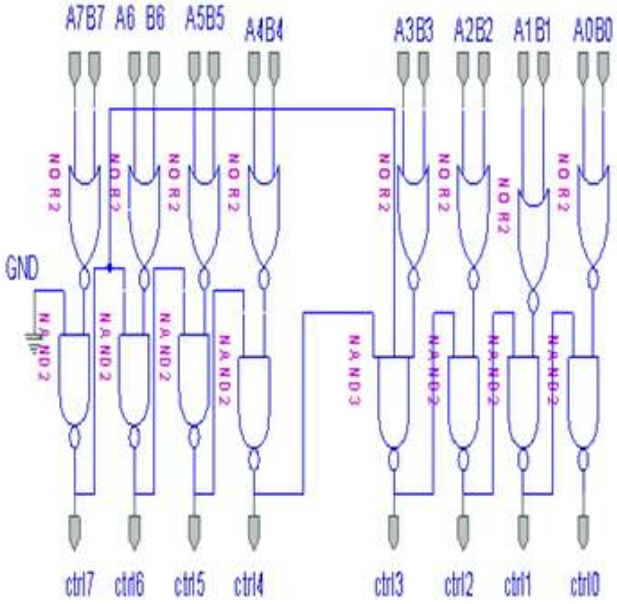

Fig. 3. Control signal producing block for 8-bit probabilistic adder

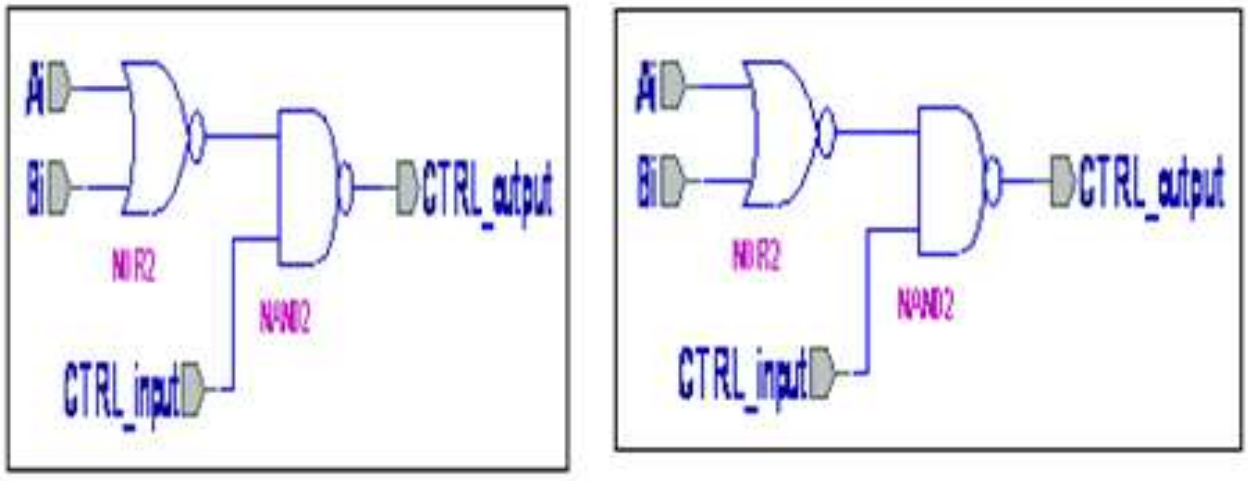

Fig. 4. Schematic implementation of control signal producing cell types

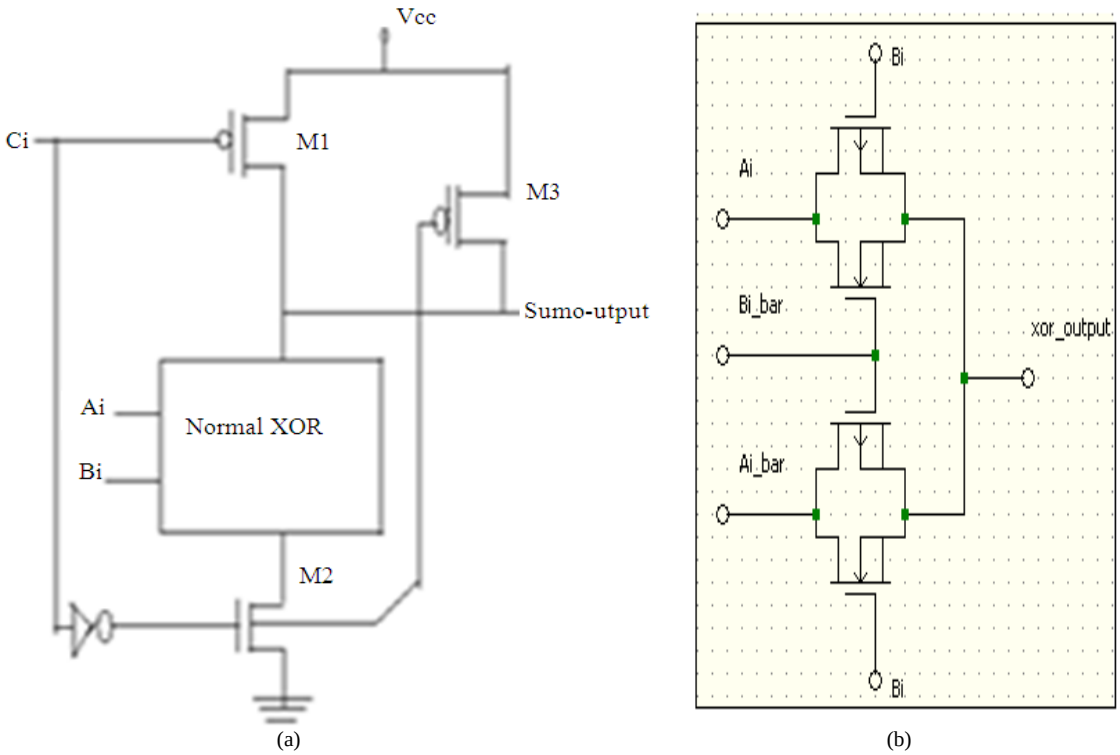

Fig. 5a and b. Advanced XOR gate and Normal XOR gate using transmission gate

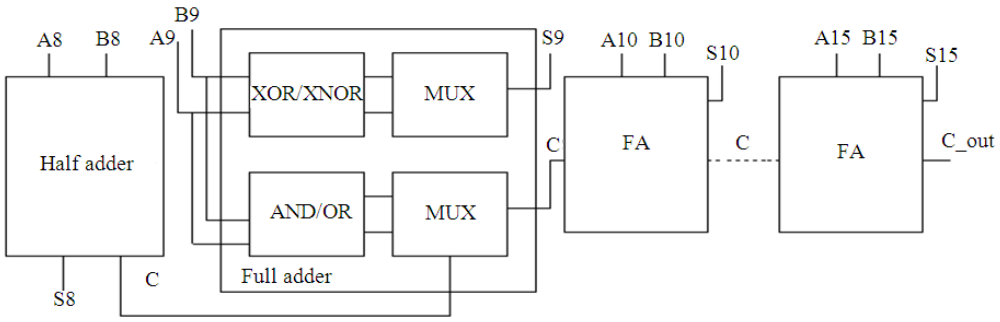

Fig. 6. Deterministic adder block using Multiplexer

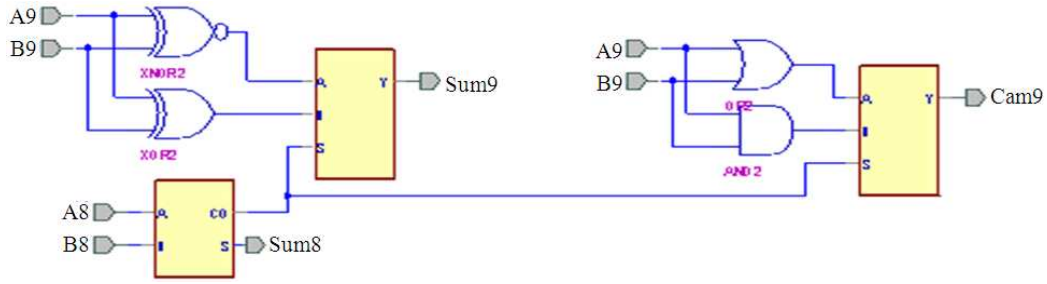

Fig. 7. Design of a single block for the deterministic full adder using multiplexer

This advanced XOR gate is consist of 3-pmos, 2-nmos and normal XOR. Both M1 and M2 in advanced XOR gate is ON when ci = 0. If ci = , then the M1, M2 is OFF and M3 is ON to produce ‘’high’ output in sum-output terminal. The proposed modification can be made by replacing the normal XOR gate using CMOS logic by transmission gates where the number of transistors can be reduced. The normal XOR gate using transmission gate CMOS logic is shown in **Fig. 5b**. Therefore transistor counts will be reduced. So the area is also been reduced.

1.3. Design of Deterministic Adder

The deterministic part is constructed using a multiplexer based adder unit. The deterministic adder block is shown in **Fig. 6 and 7**. The two inputs such as A8&B8 of this deterministic part are given in to half adder unit. Then the carry output from the half adder is used as a selection signal for two multiplexer based adder unit of next input (A9 and B9) addition process. The carry output from every previous adder block is used for selecting signal for the next multiplexer based adder block and so on. This multiplexer based adder block is used to produce the individual sum output and final carry output for deterministic part. The overall delay is determined by the deterministic part and also probabilistic part need be a fast adder. The multiplexer based adder block has been chosen for the deterministic part of the circuit. The given multiplexer in deterministic adder is constructed by using transmission gates where the number of transistors can be reduced.

2. MATERIALS AND METHODS

The proposed adder is designed in XILINX tool using VHDL code and simulated using Modelsim. HSPICE software was used to construct the models of the proposed adder and the conventional adders. 1000 sets of inputs were randomly created using the mat lab program. Designed for each position of input, on the way to run the simulation for each adder and recorded the power consumption. With 1000 set of outcome, typical power utilization was determined. The transistor count was derived openly from the HSPICE software.

3. RESULTS

The delay evaluation, power dissipation and PDP of different types of an adders are shown in **Fig. 8**. The **Fig. 9** shows that the transistor count of proposed adder compare with other conventional adders.

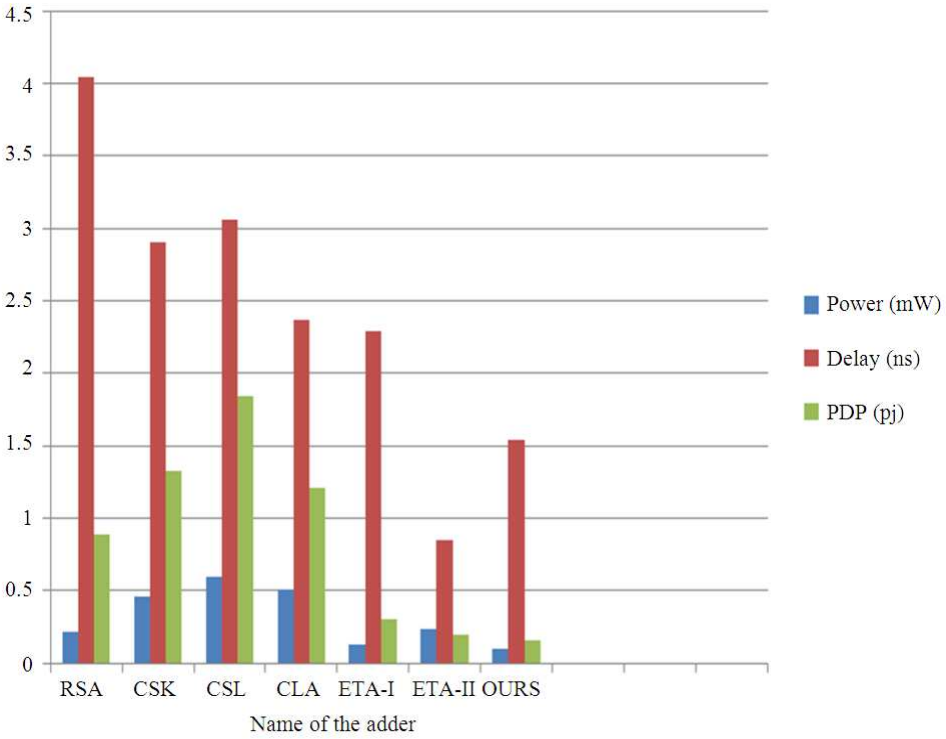

Fig. 8. Power delay product of different adders

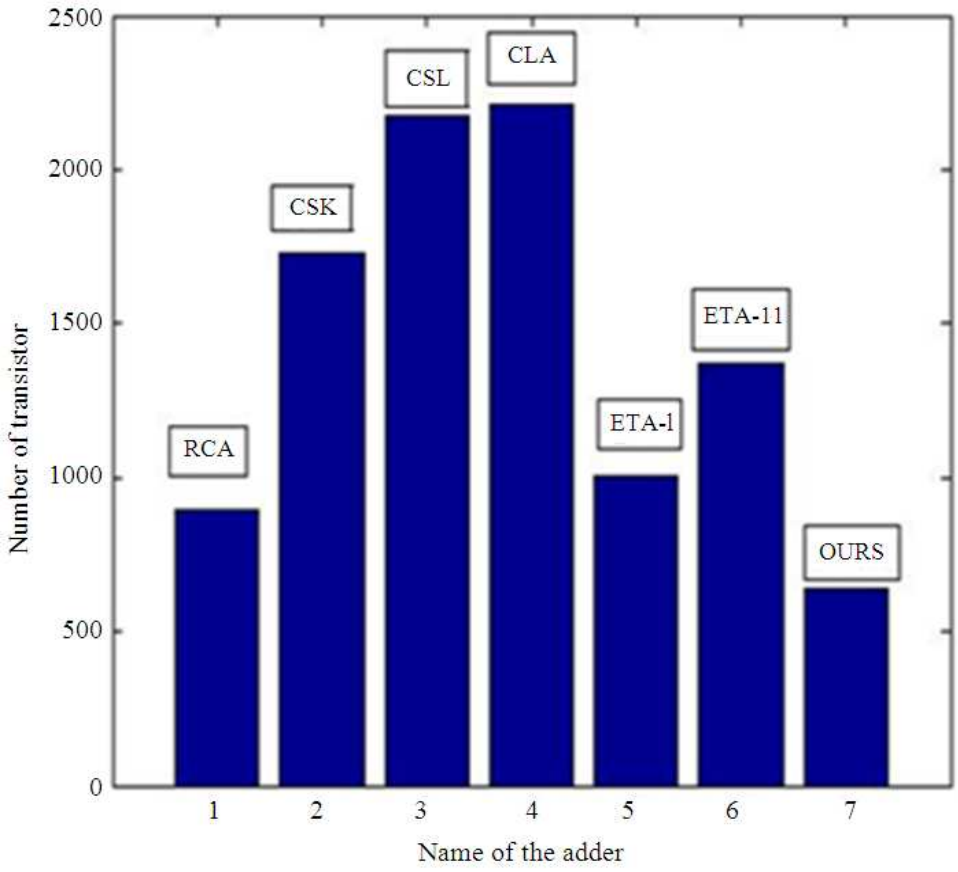

Fig. 9. Transistor count for different adders

4. DISCUSSION

To compare the output of proposed adder with actual value for 1000 number of samples, it is found that the percentage of error is 1.7 i.e., the percentage of accuracy is 98.3% Comparing the simulation results of the proposed adder with those of the conventional adders, it is evident that the proposed adder performed the best in terms of power consumption, delay and Power-Delay Product (PDP).

5. CONCLUSION

The probabilistic adder to provide a physically compact high speed and low power utilization component. The centre part of any signal processing unit, this adders are in extremely high demand on its speed and low power utilization. To reduce major power utilization of adder design it is a good direction to reduce number of computation thereby reducing a dynamic power which is a major part of total power dissipation. Simulation results illustrate the superiority of the resulting proposed adder against conventional adders in terms of power, delay and PDP. The proposed adder is mostly applicable to signal processing subsystems.

6. REFERENCES

Chong, S. and A. Ortega, 2005. Hardware testing for error tolerant multimedia compression based on linear transforms. Proceedings of the 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI System, Oct. 3-5, IEEE Xplore Press, pp: 523-531. DOI: 10.1109/DFTVS.2005.38

Hsieh, T.Y., K.J. Lee and M.A. Breuer, 2007. Reduction of detected acceptable faults for yield improvement via error-tolerance. Proceedings of the Conference on Design, Automation and Test in Europe, Apr. 16-20, ACM Press, Nice, France, pp: 1599-1604.

ITRS, 2003. International Technology Roadmap for Semiconductors. Germany.

Kim, S.H., S. Mukhopadhyay and M. Wolf, 2011. Modeling and analysis of image dependence and its implications for energy savings in error tolerant image processing. IEEE Trans. Comput. Aided Design Integr. Circ. Syst., 30: 1163-1172. DOI: 10.1109/TCAD.2011.2126573

Lee, K.J., T.Y. Hsieh and M.A. Breuer, 2005. A novel test methodology based on error-rate to support error-tolerance. Proceedings of the IEEE International Test Conference, Nov. 8-8, IEEE Xplore Press, Austin, TX, pp: 1136-1144. DOI: 10.1109/TEST.2005.1584081

Ramkumar, B. and H.M. Kittur, 2012. Low-power and area-efficient carry select adder. IEEE Trans. Very Large Scale Integr. Syst., 20: 371-375. DOI: 10.1109/TVLSI.2010.2101621

Shin, D. and S.K. Gupta, 2011. A new circuit simplification method for error tolerant applications. Proceedings of the Design Automation Test in Europe Conference Exhibition (DATE), Mar. 14-18, IEEE Xplore Press, Grenoble, pp: 1-6. DOI: 10.1109/DATE.2011.5763248

Vergos, H.T., 2012. Area-Time efficient end-around inverted carry adder. Integr. VLSI J., 45: 388-394. DOI: 10.1016/j.vlsi.2011.11.003

Weste, N.H.E. and K. Eshraghain, 2010. Principles of CMOS VLSI Design. 1st Edn., A Systems Perspective Pearson Education.

Zhu, N., W.L. Goh, W. Zhang, K.S. Yeo and Z.H. Kong, 2010. Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing. IEEE Trans. Very Large Scale Integr. Syst., 18: 1225-1229. DOI: 10.1109/TVLSI.2009.2020591