

Low Power Phase Locked Loop Frequency Synthesizer for 2.4 GHz Band Zigbee

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Abstract: Problem statement: Wireless communication systems are required for many applications. There are different standards for these systems. IEEE 802.15.4 defines the communication system standard for Zigbee. This study discussed designing one of the blocks of Zigbee transceiver which is the Phase Locked Loop (PLL). A major target for any communication systems is saving battery power, especially for Zigbee as it is meant to be a low cost communication system. Phase locked loop is responsible on carrier frequency selection in a communication system. It is the most power consumer block in the transceiver as well. The objective of this study was designing a low power fully integrated integer-N PLL frequency synthesizer targeting the 2.4 GHz band IEEE 802.15.4 Std Zigbee. **Approach:** Minimizing total power consumption of PLL was achieved by introducing a novel design of Phase Frequency Detector (PFD) and modifying the rest of the PLL blocks. The proposed PFD used only 12 transistors and it preserved the main characteristics of the conventional PFD with a simple architecture. The Charge Pump (CP) was single-ended source switch to save power and minimize mismatches. The Voltage Controlled Oscillator (VCO) spans from 4.737-4.977 GHz band using LC resonator. The VCO worked at double the frequency band to avoid local oscillator leakage and feed through. The integer N divider used a 15/16 dual modulus. **Results:** The proposed PLL was designed using Silterra 0.18 μm CMOS process. It consumed 3.2 mW with 1.8 voltage supply. Phase noise is -113.4 dBc Hz^{-1} at 1 MHz. The proposed PFD works up to 2.5 GHz with free dead zone. The Charge Pump (CP) works with 20 μA , lock-in time is 27 μs and total die area is 1×2 mm. All results were taken from extracted layout simulations. **Conclusion:** The results of this study indicated that a PLL can work with less power consumption and save the transceiver battery. The proposed PFD was suitable for high speed applications.

Key words: Phase frequency detector, charge pump, voltage controlled oscillator and dual modulus

INTRODUCTION

Wireless communication systems are widely used these days. They have many applications such as cellular phones, notebooks and wireless sensors networks. These applications aim not only a good quality of data transmission but also low power consumption. This helps in having long life battery for these applications. The transceiver in a communication system is composed of many blocks: Low Noise Amplifier (LNA), mixer, power amplifier and phase locked loop. PLL has the major power consumption among these blocks. It generates the carrier frequency for transmission and selects channel frequency for reception. Decreasing its power would decrease total power of the transceiver.

The Zigbee alliance has been developing a standard based wireless sensor networks with low data rates and

low power consumption. IEEE 802.15.4 defines Physical (PHY) layer and Medium Access Control (MAC) layer. IEEE 802.15.4 assigns three frequency bands of operation: The 868, 915 MHz and 2.4 GHz unlicensed bands. Among the three the 2.4 GHz band is highly attractive, since this unlicensed band is commonly available throughout the world. The typical applications of this low data rate standard include those for industrial and commercial uses, home automation, PC peripherals, consumer electronics and personal health care applications, as well, as toys and games that should be able to run for six months to two years on just button cells or batteries^[1].

This study presents a complete design of PLL for the IEEE 802.15.4 2.4 GHz frequency band Zigbee standard. It represents solutions for minimizing the power consumption.

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MATERIALS AND METHODS

There are different types of frequency synthesizers: the direct digital synthesizer, the direct analog synthesizer and the phase locked loop or the indirect synthesizer^[2]. Both the direct digital and the direct analog synthesizers have high power consumption for their complex architecture. PLL has relatively less power consumption and simpler architecture. This makes PLL is the most frequency synthesizer suitable for the System On Chip (SOC) in wireless communication systems. The phase locked loop frequency synthesizer consists of: phase frequency detector, charge pump, loop filter, voltage controlled oscillator and programmable divider. They are connected in a feedback loop as shown in Fig. 1. The key parameters in the PLL frequency synthesizers are phase noise, quadrature mismatch (I/Q), total power consumption and lock in time. The VCO has the major phase noise contribution in PLL. VCO's phase noise has to be within the specifications of the standard.

Some of the Zigbee system specifications for the frequency synthesizers are listed in Table 1. From these specifications the maximum tolerable phase noise by the system can be calculated by using Eq. 1^[3,4]:

$$SNR = \frac{P_{sig} + P_{LO}}{P_{int} + P_N + P_{BW}} > SNR_{min} \quad (1)$$

Where:

- P_{sig} = The power content of the carrier
- P_{LO} = The power content of the LO
- P_{int} = The power content of the interferer
- P_N = The phase noise contribution of the LO
- P_{BW} = The power content of the LO signal across the channel bandwidth

SNR_{min} = The required SNR at the input of the IF section following down conversion for the given demodulation scheme and tolerable bit error rate

Table 1: System specifications of the 2450 MHz IEEE 802.15.4 PHY layer

Performance metrics	Specifications
Carrier	2400 MHz
Spectrum	2400-2483.5 MHz
Channel bandwidth	3 MHz
Channel spacing	5 MHz
No. of channels	16 (11-26 of the PHY layer)
Sensitivity	-85 dBm
Signal to Noise Ratio (SNR)	2 dB
Alternate channel rejection	30 dB at 10 MHz offset
Adjacent channel rejection	0 dB at 5 MHz offset
Output transmitted power	-5 to 3 dBm
Transmission data rate	250 Kb sec ⁻¹

Assuming 10 dB for the non-ideality of the system, the phase noise specification of 10MHz offset from the carrier is -110 dBc Hz⁻¹. The reference frequency Fref equals the channel spacing 5MHz to control the step of the integer-N.

The blocks of the PLL frequency synthesizer are designed as follows:

Phase Frequency Detector (PFD): The main concept of PFD is comparing 2 frequency inputs in terms of both phase and frequency. These frequency inputs are reference frequency (Fref) and output of voltage controlled oscillator after Division (Fdiv). The output is a pulse represents the difference between the inputs and drives the charge pump to increase the control voltage or decrease it or keep it constant without change^[5]. A PFD is usually built using a state machine with memory elements such as D-FF. The proposed PFD in this study Falling Edge PFD (FE-PFD) reduces the power consumption by using simple architecture composed of only 12 transistors as shown in Fig. 2. When both Fref and Fdiv are low, UPb and DNb start precharging then UP and DN go low. Both UP and DN go high when both Fref and Fdiv are high. At the falling edge of Fref, DNb starts precharging and DN goes low. Up goes low following the falling edge of Fdiv. The difference in pulse width between UP and DN signals represents the difference in the input phase.

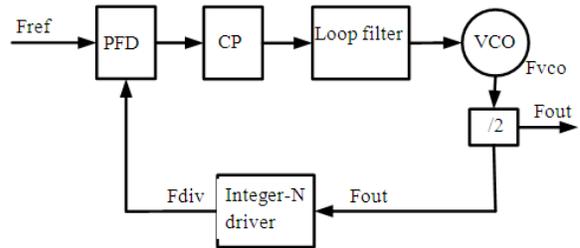


Fig. 1: Fundamental PLL

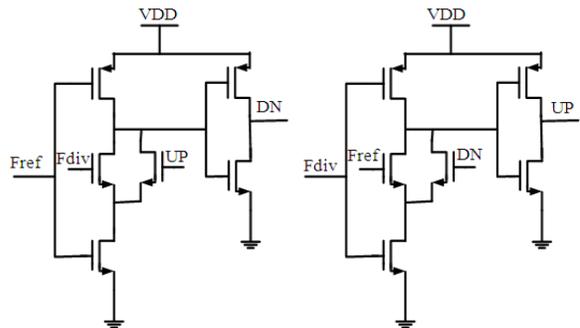


Fig. 2: Proposed PFD (FE-PFD)

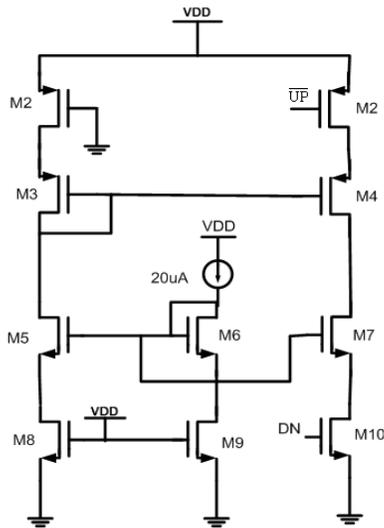


Fig. 3: Proposed charge pump architecture

Charge pump: The role of a charge pump is converting the digital signal output from a PFD into analog signal. A charge pump consists of two switched current source. It either source (I_{up}) or sink (I_{dn}) current according to UP and DN signals. It is important that the current mismatch between I_{up} and I_{dn} is reduced^[6]. The current mismatch is minimized in this design by ensuring that the current source is same as the current sink, thus experiencing the same process variations. The schematic of the proposed charge pump is shown in Fig. 3. The charge pump designed is single-ended source switch architecture. It is chosen for its simplicity, high speed and low clock feed through. Switches M1 and M10 are controlled by the PFD outputs (UP and DN). The current mirrors formed by transistors M5, M6 and M7 as well as M3-M4 pair ensure equal amount of current for UP and DN branches. Transistors M2, M8 and M9 are included to act as dummy switches to reduce timing mismatch. The current source in this design is chosen such that the current produced is 20 uA.

Voltage controlled oscillator: The role of VCO is generating the required carrier frequency for each channel. Complementary differential oscillator is used for designing the VCO as it depends on the idea of current reuse to save power consumption. Since the current is fully switched from one side to the other, then it makes sense to provide that current through a commutator switch operating on current source of half that required for a regular current biased oscillator as shown in Fig. 4^[7,8]. The VCO spans from 4.737-4.977 GHz band using LC resonator.

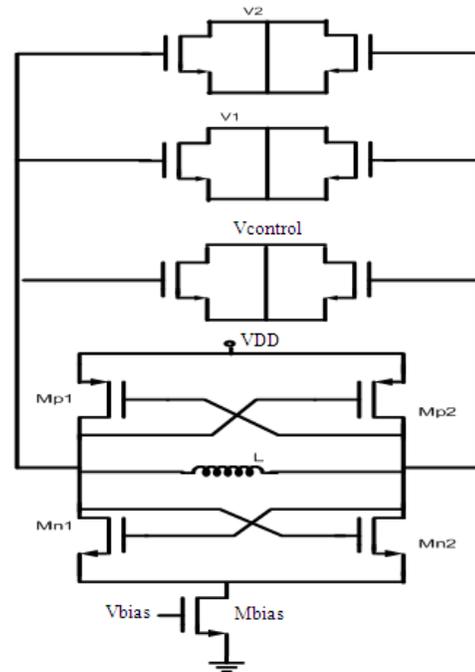


Fig. 4: Complementary differential VCO

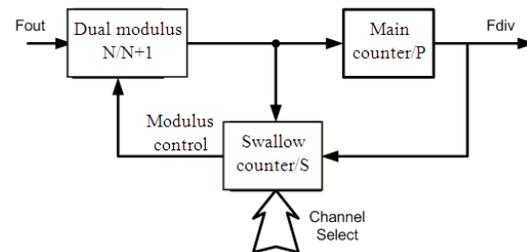


Fig. 5: Integer-N architecture frequency synthesizer

The VCO works at double the frequency band to avoid local oscillator leakage and feed through.

Integer-N programmable divider: Integer-N divider in a PLL is responsible on channel selection. It divides the output frequency “Fout” with certain value according to the channel number, to be compared with reference frequency by Phase Frequency Detector. The integer-N consists of a dual modulus prescaler with division ratio $N/N+1$ and two programmable down counters as shown in Fig. 5. The main counter “P” and swallow counter “S”, where $S \leq P$. The swallow counter is loaded by 4 bits externally to select the required channel. The control modulus signal is set to “high”, the prescaler divides by $N+1$. Since the output of the prescaler is the input clock of both P and S counters, then they down count by $F_{out}/(N+1)$ frequency until swallow counter reaches zero. The

control modulus signal is set to “low”, the prescaler divides by N. The main counter continues down counting with input clock F_{out}/N until it reaches zero. After the two counters are reset, the process begins again^[9,10]. The output frequency F_{div} can be expressed as a function of the input frequency F_{out} as follows:

$$F_{div} = [S(N+1) + (P-S)N] F_{out}$$

Considering a frequency synthesizer for the Zigbee IEEE Std 802.15.4 standard, the values of P, S and N are calculated as follow: The frequency band has 16 channels represented by 4 bits. The channel spacing is 5 MHz. the frequency band is 2400-2480 MHz then:

- The prescaler dividing factor is 15/16 (N = 15)
- The main counter P is 32
- The swallow counter has a value in between 0-15

The dual modulus design is shown in Fig. 6. The three input NAND gate has Mode, $\overline{Clk8}$ and $\overline{Clk16}$ signals as inputs. When the three signals are high,

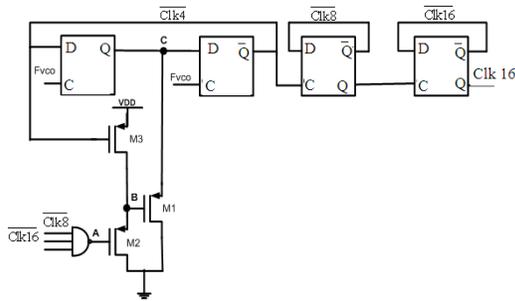


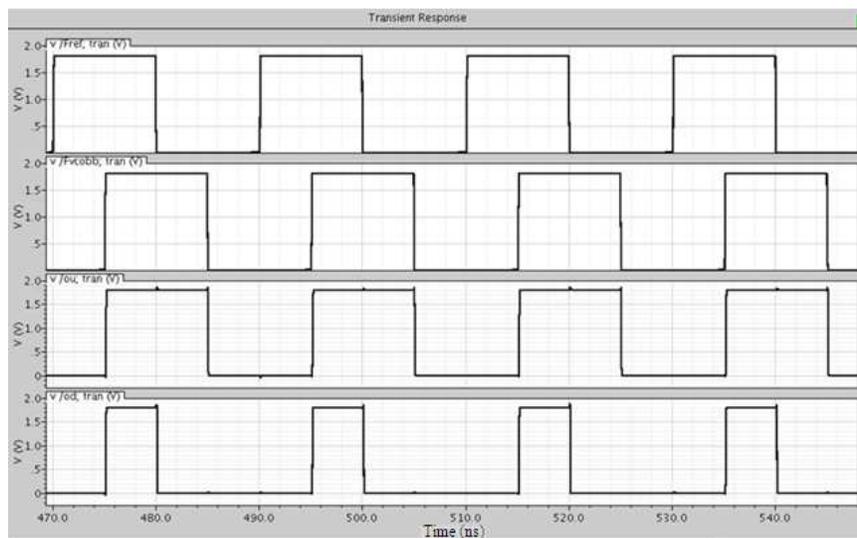
Fig. 6: Dual modulus architecture

the NAND output “A” is low which results in turning off M2 and charging up node B through M3 to turn ON M1. M1 pulls down the node C causing the counter to divide by 3 and the total output would be divided by 15.

When the Mode signal is low, the NAND output “A” is high and M2 is turned ON. This discharges node B causing M1 to turn OFF. With M1 is OFF no pull-down for node C. Therefore, the DFF will operate normally and divide by 4 and the total output would be divided by 16. The critical path is from $\overline{Clk16}$ to node C through M3 and M1. This means the delay in critical path is rather small and the load from critical path and high frequency node $\overline{Clk16}$ is comparably low. This structure results in high speed and minimum power consumption for less number of FFs and logic gates.

RESULTS

All results in this study are based on simulations of extracted layout using Spectre, the voltage supply is 1.8 V. The layout was made using Silterra 0.18 um CMOS process. The timing diagram of the FE-PFD at case of locking and at the case where F_{div} lags F_{ref} are shown in Fig. 7. FE-PFD works up to 2.5 GHz at 1.8 V. VCO tuning bands are shown in Fig. 8. The quadrature outputs are matched as shown in Fig. 9. Phase noise of VCO is -113dBc/Hz as shown in Fig. 10. The control voltage, PLL output, DN and UP signals respectively are shown in Fig. 11, they show locking process of the proposed PLL. The layout of the proposed PLL is shown in Fig. 12.



(a)

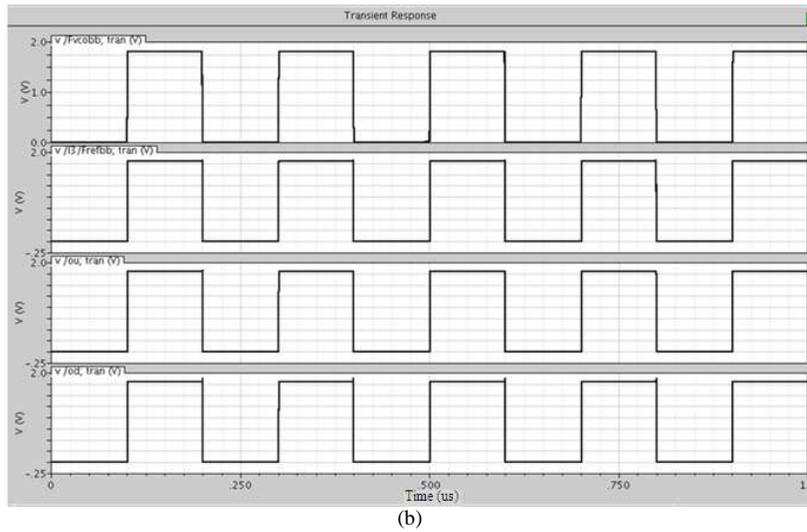


Fig. 7: FE-PFD timing diagram simulated at 50 MHz (a): At 5nS delay, (b): At locking

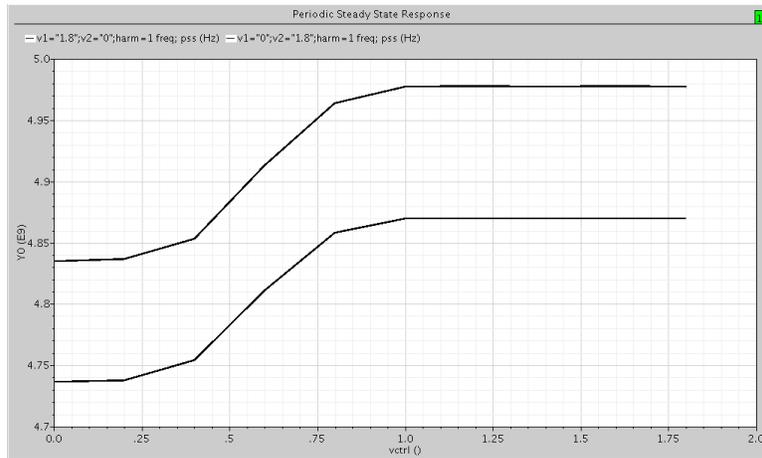


Fig. 8: Sub-bands covered by VCO

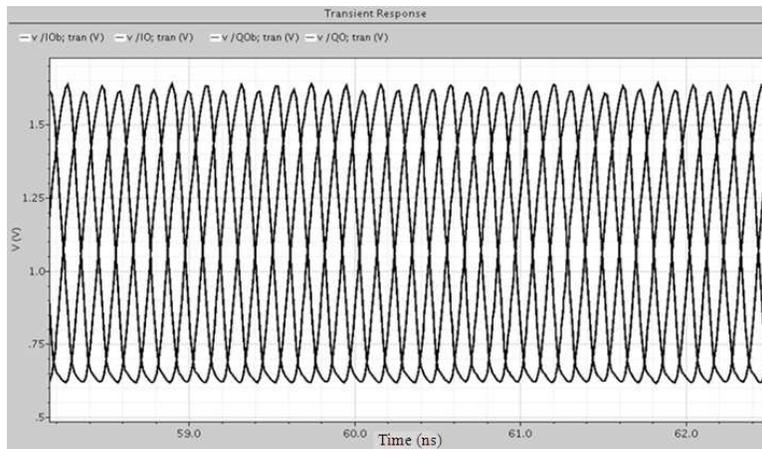


Fig. 9: Quadrature output of PLL

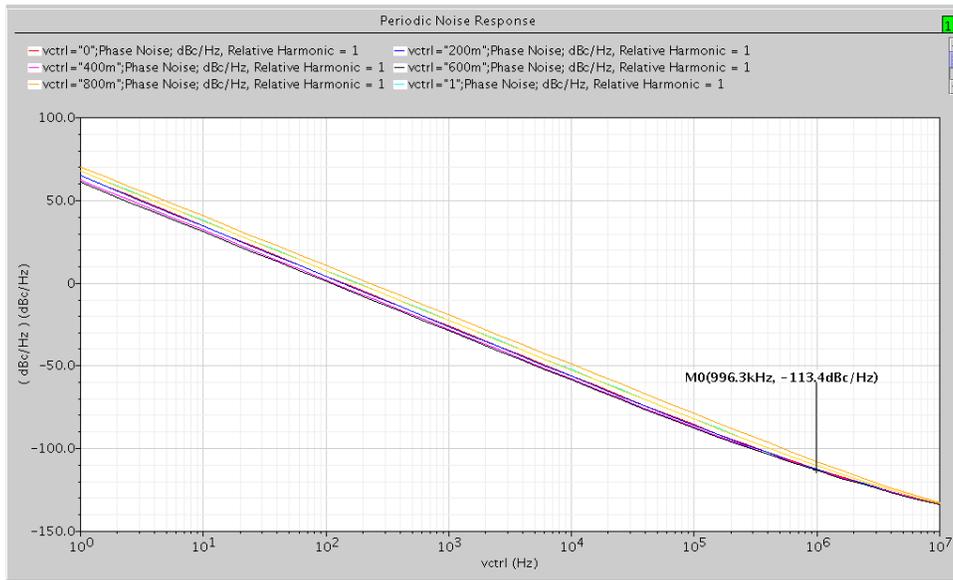


Fig. 10: Overall phase noise of proposed PLL

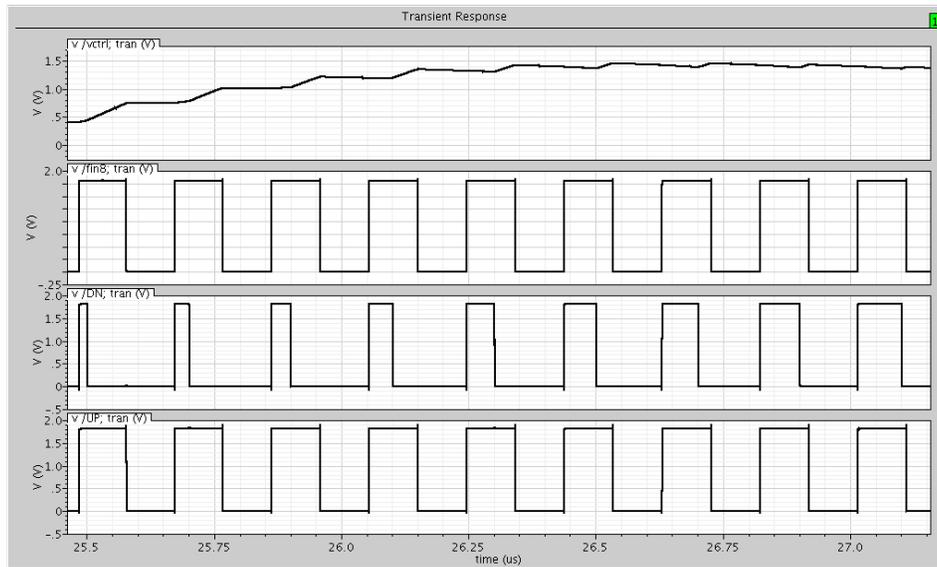


Fig. 11: Lock-in process of third order PLL where FE-PFD is used as a phase frequency detector

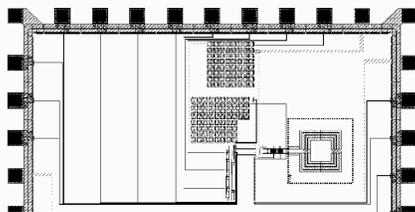


Fig. 12: Proposed PLL layout

DISCUSSION

FE-PFD can be used in other high speed applications. It has free dead zone so it can detect any phase difference between the frequency inputs. The phase noise of the VCO depends on the quality factor of the resonator. The inductor has quality factor of 10 at the required band. The VCO is covering the band by dividing it into 2 sub-bands to achieve better VCO gain

and fine tuning. The quadrature output is generated by dividing the output of VCO by 2 i.e., no extra quadrature generation circuit is needed.

There is no I/Q phase mismatch in the output.

CONCLUSION

This study proposed a CMOS PLL frequency synthesizer targeting the IEEE 802.15.4 standard for Zigbee. It has low power consumption of 3.2 mW. A novel design of phase frequency detector is proposed. Minimizing the overall power of PLL is done by minimizing power of each individual block and applying different techniques for each. It is implemented using Silterra 0.18 um CMOS process. All results are taken from extracted post layout simulations.

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REFERENCES

1. Oh, N. and S. Lee, 2006. Building a 2.4 GHz radio transceiver using IEEE 802.15.4: IEEE Circ. Devices Mag., 21: 43-51. DOI: 10.1109/MCD.2005.1578587
2. Egan, W., 1999. Frequency Synthesis by Phase Lock. 2nd Edn., John Wiley and Sons, Inc., New York, ISBN: 0-471-32104-4, pp: 14-27.
3. Razavi B., 1998. RF Microelectronics. Prentice Hall PTR, Printice-Hall Inc., Upper Saddle River NJ 07458, USA., ISBN: 0-13-887571-5, pp: 247-296.
4. Aktas, A. and M. Ismail, 2004. CMOS PLLs and VCOs for 4G Wireless. Kluwer Academic Publishers, USA., ISBN: 1-4020-8060-3, pp: 12-40.
5. Best, R.E., 2003. Phase-Locked Loop Design, Simulation and Application. 5th Edn., McGraw-Hill Companies, New York, ISBN: 0-07-141201-8, pp: 7-51.
6. Razavi, B., 2003. Design of Integrated Circuits for Optical Communications. McGraw-Hill Higher Education, USA., ISBN: 0-07-282258-9, pp: 244-286.
7. Ham, D. and A. Hajimiri, 2000. Design and Optimization of a low noise 2.4 GHz CMOS VCO with integrated LC tank and MOSCAP tuning. Proceeding of the IEEE International Symposium on Circuits and Systems, May 28-31, IEEE Xplore Press, Geneva, Switzerland, pp: 331-334. DOI: 10.1109/ISCAS.2000.857097
8. Hegazi, E., J. Rael and A. Abidi, 2005. The Designer's Oscillator Guide to High Purity Oscillators. Kluwer Academic Publishers, USA., ISBN: 1-4020-7666-5, pp: 240.
9. Leenaerts, J.V.D. Tang and C.S. Vaucher, 2001. Circuit Design for RF Transceivers. Kluwer Academic Publishers, USA., ISBN: 0-7923-7551-3, pp: 285-297.
10. Arguello, A., Joao and W. Noiye, 2005. A 3.5 mW programmable high speed frequency divider for a 2.4 GHz CMOS frequency synthesizer. Proceedings of the Integrated Circuits and Systems Design, 18th Symposium, Sept. 4-7, IEEE Xplore Press, Florianopolis, pp: 144-148. DOI: 10.1109/SBCCI.2005.4286847