

## Modelling of Digital Assisted Backend Correction Analogue to Digital Converters with Verilog-A

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**Abstract: Problem statement:** Pipelined architecture is considered to be the most suitable for high-speed and high-resolution applications among various Nyquist Analogue to Digital Converters (ADCs) in nowadays digital signal processing domain. But the pipeline power consumption is growing with the technology scaling. For a pipeline ADC with high speed and high resolution, the fore-end track and hold amplifier and residual amplifier occupies the most power consumption of the whole system, so new and novel methods is needed to lower the amplifier power consumption. **Approach:** Different from the traditional use of close-loop amplifier, open-loop amplifier is used as the first-stage residual amplifier, which greatly decreases the system power consumption and design difficulty. To correct the nonlinear error introduced by the open-loop amplifier, backend digital correction is applied. To validate the rationality and correctness of the method and confirm the design parameters, Verilog-A is used to build a behavioural model, Cadence simulation tool Spectre is used to get the result. **Results:** From the simulation result of the behavioural model, we get the Differential Nonlinearity (DNL) of the digitally backend correction ADC is  $-0.25\sim 0.25$ , Integral Nonlinearity (INL) is  $-0.5\sim 0.25$ , Spurious Free Dynamic Range (SFDR) is 77.8dB. The Total Harmonic Distortion (THD) of the system after correction is calculated to be 73.66dB, so the Effective Number of Bits (ENOB) of the is 11.78 bits. **Conclusion:** Digitally assisted backend correction is a novel approach to lower the power consumption of pipeline ADCs, which makes great significance in mixed signal system design. The use of open-loop amplifier instead of traditional closed-loop amplifier can effectively decrease the design difficulty and design process than before. Only the first stage residual amplifier is changed to open-loop in this article and this substitution can also be replicated in the track and hold circuit and the succeeding stages.

**Key words:** Digital assisted backend correction, open-loop amplifier, Verilog-A modelling, pipeline ADC, hold circuit, power consumption, Total Harmonic Distortion (THD), Differential Nonlinearity (DNL), Spurious Free Dynamic Range (SFDR), Effective Number of Bits (ENOB), Analogue to Digital Converters (ADCs)

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### INTRODUCTION

In deep submicron integrated circuit design and manufacture, digital signal processing develops fast, which makes higher speed and higher resolution ADCs necessary. The research of high resolution, low power consumption ADCs becomes one of the most popular issues recent years. There are several kinds of high quality ADCs, for example, successive approximation ADC, sigma-delta ADC, flash ADC and pipeline ADC. Among these, pipeline ADC has high speed, high resolution and fairly low power consumption and chip area.

In communications, signal processing and other applications that occupy the market, pipeline ADC continues to be the architecture of choice for high sample rate and high resolution analogue to digital converters. The higher sample rates certainly require small capacitive loads and small parasitic, which requires to improve the technology precision. Smaller device sizes inevitably lead to poor matching and thus limit the enable effective resolution. On the other hand, the trend in the market place is clearly presenting the needs of very high speed, high volume, low cost ADCs in both stand alone and integrated applications. However, the conversion rate of the ADC is limited by the growing power consumption comparing with the

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lower source voltage. The resolution of pipeline or multi-step flash ADC is usually limited by the gain of the op-amps used in the track and hold circuit and inter-stage residual amplify circuit. The higher the resolution of the ADC is, the higher the quality of the op-amp is required. Most important, the high-gain, fast-settling op-amps usually consume most of the power and the chip area of the whole system.

In traditional pipeline ADC, close-loop amplifier used in the for-end sample and hold circuit occupies a large part of the system power consumption and also, the amplifier seems to be most susceptible to integrated circuit technology scaling (Murmman and Boser, 2004). At the same time, mismatches caused by manufacturing error may also result in decreased accuracy of the circuit, thus high-performance pipelined ADC is more difficult to implement. In order to reduce adverse effects to analogue circuit, a new design methodology has been proposed and widely used, which is used as substitute the op-amps from closed-loop to open-loop. To remedy the nonlinearities caused by the open-loop amplifier, self-calibration in digital domain is used. ADC calibration techniques in digital domain can make full use of the computing power of digital circuits. Because all the ADC output is digital, it can carry out operations in the digital domain to compensate for non-ideal characteristic. Designs of pipeline ADCs have relied on high-gain operational amplifiers and excellent capacitor matching in order to produce moderate-resolution converters.

In this study, open-loop amplifier is used in a 12-bit 40MSPS digitally assisted backend correction pipeline ADC to compress system power consumption and decrease design difficulty. The whole system is modelled with hardware description language Verilog-A and simulated with Cadence Spectre simulator.

#### **Behavioural modelling and Verilog-A language:**

Concise modeling may perhaps be the most crucial part of an analog or mixed signal system design. If ignore the quality of the latency simulator algorithms, the accuracy of the results will be mainly limited by the quality and applicability of the models chosen. In the uses before, models were mainly a fixed set, built-in and compiled directly into the simulator, which makes it not flexible enough to introduction of new models and new structure into the simulation platform. Even this can be achieved on the cost of more difficulty and expense more time, such mechanisms were often non-standard, non-portable and inefficient. The lack of standardized interfaces, along with the proprietary nature of commercial simulators, led to an environment where the rapid development of portable models was not possible (Trojanovsky *et al.*, 2005).

Behavioural simulation is more and more used to explore design-space while restricting simulation time as technology size compresses and design complexity grows. In this respect, the traditional language and simulation tools adhere to it can't suffice the development of analogue and analogue mixed signal circuits effectively. To get realistic estimates of performance, Verilog-A language is employed as the platform of choice for the characterization of complex SoC (system on chip) designs and fast becoming a necessary step between system modelling and the real circuit.

The appearance of analogue hardware description languages over the past few years offers the promise of a comprehensive solution to the analog modelling and deployment problem. Verilog-A is a high-level language developed to establish the structure and behavior model for analog and mixed signal systems. It is considered an extension of the IEEE 1364 Verilog HDL specification for digital design. It is a kind of hard ware description language special for analogue circuit and analogue mixed signal circuit design.

The analog systems are described in Verilog-A as all kinds of modular with hierarchy and different levels of modeling complexity. The motivation to exploit this language is to offer a new higher level of abstraction in analogue circuit and analogue mixed signal circuit design. It has the flexibility to model blocks at different levels of abstraction and runs in a widely used Analog Design Environment (ADE).

Before the widely use of Verilog-A language, MATLAB or other language tools were often used for analogue and mixed signal circuit Behavioural modelling. As analogue systems are described in the way of blocks, called modules, it can specify the structure of the overall system or the behavioural of the relative parts. Hierarchy is created as modules inside modules. MATLAB or other language tools, which are not specified for circuit design, can't describe circuit precisely and can't apply simulation tools conveniently. The model designed in Verilog-A can be directly simulated with many commercial SPICE-based simulation tools such as Spectre, Hspice and other tools.

Through the practice of simulation, behavioural modelling with Verilog-A for analogue circuit can greatly avoid the uncertainty in directly circuit design, decrease simulation time and shorten the design process. Verilog-A is specified for the modelling of analogue circuit and in this hardware language, the properties and non-ideal elements can be precisely described, so the precision of the simulation can be greatly improved. Verilog-A provides us with a lot of hierarchies of behaviour model and many module description functions. Except for the common mathematic functions, there are special functions, along with correction definition. To make the modelling closer to the factual design, delay and noise. Can also be added to the model.

**The original of digitally backend calibration:** The rigor analogue circuit design fact characterised by lower technology dimension and low supply voltage force the designers to explore new calibration methods to compensate for the errors that are either new produced or recently become important, such as nonlinearity in the amplifier. The calibration technique can be fundamentally classified into two kinds: Analogue domain calibration and digital domain calibration. The digital domain calibration does not need extra analogue circuits such as Digital to Analogue Converters (DACs) in contrast to the analogue domain calibration and can be implemented by employing only additional digital calibration circuits to conventional pipelined ADCs. However, error measurement needs to be performed periodically depending on temperature variations and supply voltage variations. Although some background calibration techniques can remove this problem by simultaneously performing device error measurement and elimination in normal mode, extra circuits for error measurements in background such as highly accurate delta-sigma converters result in other overhead cost of increased chip area and power consumption (Wang *et al.*, 2004).

The concept of digital assisted backend correction pipeline ADC was described in detail by Boris Murmann in the book digital “assisted pipeline ADCs” and the use of open-loop amplifier was bring up earlier. The digital-domain calibration can be applied to more than one stage starting from the first stage of multistage pipelined ADCs. In multistage calibration, error measurement should be processed from the back-end stage to the front-end stage of the calibrated stages sequentially to measure the front-end stage errors precisely by eliminating the back-end stage errors.

**Digitally assisted calibration system:** In this study, a 40 MHz, 12 bit digitally backend correction pipeline ADC is used as prototype and the whole system is modelled in Verilog-A language. To decrease the complexity of the circuits and the design requirement of the sub blocks, the backend correction scheme is applied only in the first and least significant stage. The structure of the system and the idea of digitally assisted calibration are illustrated Fig. 1. We can see that the system can be departed into several parts partitioned by function. The first stage sub-ADC (3 bits), random codes producer, open-loop amplifier, backend ADC, error compensation cell and hyperbolic remainder curve distance estimation cell.

The residual amplifier of the first stage is changed to open-loop and causes nonlinearities to the following stages, which will engender code missing.

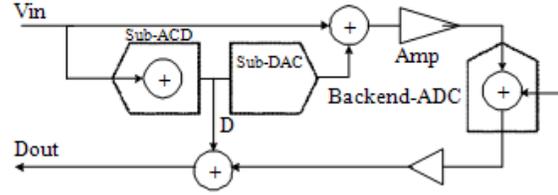


Fig. 1: Architecture of Digital assisted pipeline ADC

Digital calibration is to adjust the digital domain variable  $D_b$  correspond to the first stage analogue domain residual  $V_{res}$ , which is added by non-ideal elements. The non-ideal is measured by backend ADC along with the actual value. After calibration, the gain slope error still exists, but the ADC transfer function is linear. Digital calibration increases the complexity of digital circuitry, but the overhead is quite small in deep sub-micron CMOS process.

Because of the open-loop amplifier, nonlinear error is introduced into the system. To correct the nonlinearities,  $e(D_b)$  is added to correct the nonlinearities, the expression of  $e(D_b)$  is calculated to be Eq. 1:

$$e(D_b) = D_b - 2\sqrt{\frac{-b_1^3}{3b_3}} \cos \left[ \frac{\pi}{3} + \frac{1}{3} \cos^{-1} \left( \frac{D_b}{2\sqrt{\frac{-b_1^3}{27b_3}}} \right) \right] \quad (1)$$

In this study, the gain error of the open-loop amplifier, INL, DNL and SFDR of the ADC are simulated by Cadence Spectre.

## MATERIALS AND METHODS

Modelling of open-loop amplifier : As we know that we can achieve a compact third order nonlinearity model by appropriately choosing the gate overdrive of the open-loop amplifier, so we consider the case when the transfer function of the open-loop amplifier can be expressed as Polynomial.

The transfer function of the open-loop amplifier is showed in Eq. 2:

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \quad (2)$$

In this design, we have three bits in the first stage, so the gain of the open-loop amplifier is chosen to be 8 and the transfer function of the amplifier is polynomial. The key to design the amplifier is to construct the polynomial model. Figure 2 gives the simulation result of the amplifier model.

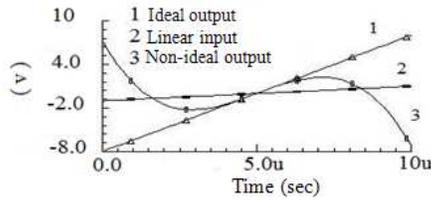


Fig. 2: Linear and non-linear amplifiers output

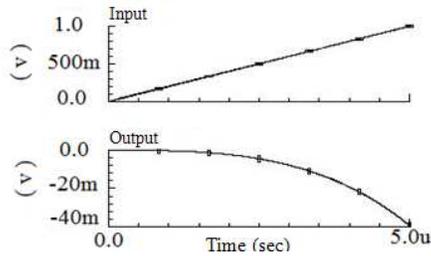


Fig. 3: Output of the compensation model

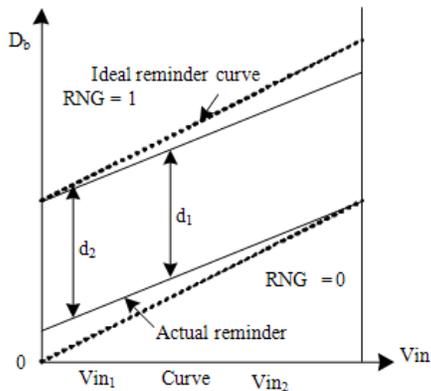


Fig. 4: Non-ideal Hyperbolic remainder curve

**Establishing of hyperbolic remainder curve:**

Random codes is needed to be added to the output of the first stage sub-ADC, we get a group of hyperbolic remainder curve from the output of the open-loop amplifier. One bit random code is created by random codes generation function. The period of the random codes in this design is chosen to be 128 bits, the time to produce one code is half of a clock circle.

Modelling of compensation function : The compensation function  $e(D_b)$  is used to correct the nonlinear errors introduced by the open-loop amplifier. In this cell, we first transform the voltage input into real constant, do mathematic operation and export voltage signal. Figure 3 give the output of the  $e(D_b)$  cell, the input is chosen as linear, the range is 0V~1V.

**Parameter estimation circuit modelling:** The majority background calibration is based on the statistical method. Because of the existence of the nonlinearities introduced, when import random codes to the lowest bit of the first stage sub-ADC output, the curve exported from open-loop amplifier is not an exact hyperbolic curve, there is distance in the vertical direction from the ideal curve (Huayu *et al.*, 2004), we can get evidence from Fig. 4.

The relationship between the distance and parameter  $k_3$  and  $k_{3opt}$  can be expressed by Eq. 3. There into,  $k_3$  is one of the parameter we need to estimate (Murmman and Boser, 2004),  $k_{3opt} \approx a_3/a_1^3$ . From Eq. 3, we get that: when  $d_1=d_2$ ,  $k_3=k_{3opt}$ , the effect of the correction works the best (Murmman and Boser, 2004):

$$\Delta d = d_1 - d_2 = 3b_1^3 \Delta \cdot (k_3 - k_{3opt}) \cdot [(V_{d1} - V_{d2})(\Delta - (V_{d1} + V_{d2}))] \quad (3)$$

**Modelling of distance estimation:**

In order to calculate the distance of the hyperbolic remainder curve, we need distance estimation circuit. Distance estimation circuit is used to count and calculate  $D_b$  in Fig. 4. Acquire the distance of the certain two points in the curve  $d_1$  and  $d_2$ , get there difference  $\Delta d$ . in the course of A/D conversion, the parameters in  $e(D_b)$  updates and optimizes, until  $\Delta d = 0$ . We get the best approximation of  $a_1$  and  $a_3$ . All the correction parameters rely on the distance estimation module, so correctly modelling of distance estimation is crucial in the whole system. When the input is  $v_{in1}$ , calculate the times code “0” and code “1” appears, we mark his two numbers as “m” and “n”. when  $m = n$ , that means “0” and “1” appears almost the same times, we get the value of both outputs  $y_1$  and  $y_2$ , get the difference  $d_1 = y_1 - y_2$ . For input  $v_{in2}$ , we do the same operation, get  $d_2$ . Subtract  $d_2$  from  $d_1$  we get  $\Delta d = d_1 - d_2$ . In the ideal case, when the third and higher order nonlinearity equals zero,  $\Delta d = 0$ . Apply this cell for two times, we get  $\Delta d$ , write a cell to judge  $\Delta d$  equals zero or not. If  $\Delta d$  equals zero, the compensation function can compensate the nonlinear error to the biggest range.

**RESULTS**

Figure 5 gives the simulation result of the digitally correction pipeline ADC system. We can see that before correction, DNL is -0.5~0.5, INL is -18.5~0.5, SFDR is 36.2dB. After correction, DNL is -0.25~0.25, INL is -0.5~0.25, SFDR is 77.8dB. From the result, we get THD of the system after correction is 73.66dB, so the ENOB of the is 11.78 bits, so we can prove the digitally correction method for pipeline ADC is correct and effective and Verilog-A modelling before circuit design is necessary.

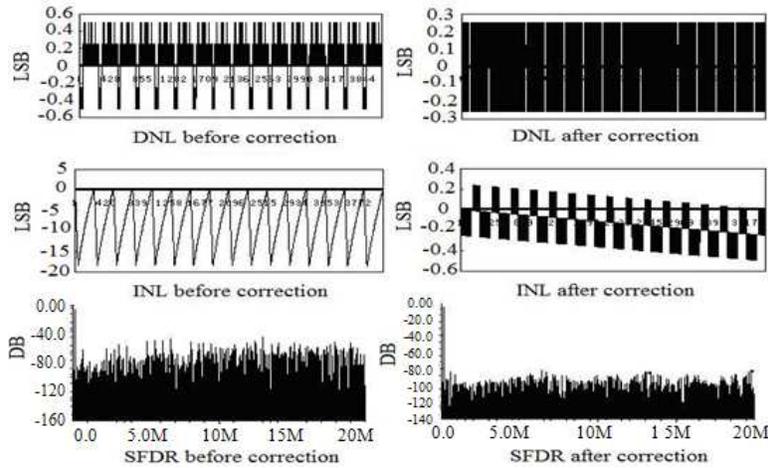


Fig. 5: DNL INL SFDR before and after correction

**DISCUSSION**

For digitally assisted backend calibration, the calibration accuracy is not limited by the remaining conversion stages. The mathematical principle behind this approach could be applicable to a wide range of ADC architectures including successive approximation and even flash types. This technique can be extended to the track and hold amplifier and the other stages and also, the calibration scheme can be employed to correct the nonlinear errors in closed-loop amplifiers.

**CONCLUSION**

Modelling with Verilog-A before circuit design can greatly improve the design validity and decrease the simulation time. It indeed represented a suitable environment for the fast estimation and realization of new compact modelling ideas. It will also be employed for implementation.

This study expands the digital-calibration theory developed and derives a novel background digitally calibration scheme custom-tailored for pipeline ADCs. By the use of open-loop residual amplifier, nonlinear error is introduced into the pipeline ADC, compensatory function is applied to complete the correction. Random codes added, engender hyperbolic remainder curve after open-loop amplifier. Estimation circuit estimate and calculate the distance between hyperbolic curve, get the parameters needed for the correction, gradually optimize design until get the optimal value.

A new background calibration technique for pipelined analogue to digital converters is proposed. By adding a group of random codes into the lowest bit of the sub-ADC output, it is possible to calibrate a pipeline stage without interrupting the normal analogue to digital

operation. The calibration can compensate the nonlinear effects introduce by the open-loop residual amplifier in the analogue to digital conversion. From the simulation result, the ENOB reaches 11.78 bits. The calibration scheme is effective to concise the system power consumption, which offers a new executable way to improve the design quality of pipeline ADCs. Verilog-A language plays a role of a convenient tool and good auxiliary way for analogue and mixed signal circuit design.

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