American Journal of Applied Sciences

Review

Architecture of an Ultra-Low-Power Fully Autonomous Universal Power Conditioner of Energy Harvester for Wireless Sensor Networks: A Review

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Article history
Received: 24-05-2015
Revised: 25-09-2015
Accepted: 26-03-2016

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Abstract: A fully autonomous Universal Power Conditioner (UPC) that can accept energy from any micro-energy harvester (e.g., photovoltaic, thermoelectric, electromagnetic, piezoelectric etc.) is proposed. Generally, UPC removes the need of multiple optimized source specific converters. But, the proposed UPC architecture will be Ultra-Low-Power (ULP) with maximized efficiency to support the low energy levels generated by harvesting sources. This UPC uses a universal source detection block consisting of source converter block, boost converter, storage unit and buck regulation. A voltage threshold block reduces the energy processing stage. A kick-start circuit enables self-starting operation. A power management block achieves efficiency in energy storage and charge cycles. The UPC will be modeled, designed and simulated in PSPICE. A behavioral model will be designed and simulated on Modelsim. The UPC will be realized on FPGA board, validated and analyzed in layout using 0.13 µm CMOS process technology. The expected result is a feasible arbitrary input source detector capable of 2-3 different sources with minimum 1 mW output power for WSN nodes or charging battery sets. The power converters are expected to consume <100 µW at >90% peak efficiency with input dc voltage at 0.02-5 V and output dc voltage from 0.5-5 V.

Keywords: Universal Power Conditioner (UPC), Ultra-Low-Power (ULP), Energy Harvesting Chip, Universal Source Converter, Power Management

Introduction

Energy harvesting also known as energy scavenging dates back to the days of windmills, waterwheel and waste heat when batteries and dynamos were yet to be invented by Volta in 1799 and Faraday in 1831 respectively. Energy harvesting captures and stores renewable energy sources by employing interface circuits, storage devices and other power management units (Khaligh and Onar, 2009).

Energy is of utmost importance to the human civilization in every possible way. Therefore, the inevitable future exhaustion of our principle energy source (petroleum) must be addressed promptly. This leads to an accelerated interest in renewable energy harvesting. Unlike conventional electrical power generation systems, energy harvesting does not use fossil fuels thus significantly reducing air pollution in the process. Moreover, the motivation for the Internet of Things (IoT) and to drive low power electronics such as Wireless Sensor Networks (WSN) and mobile devices via green and environmentally friendly resources gave rise to advanced technical methods that were developed to increase energy harvesting efficiency mechanically (Kong *et al.*, 2014) or via its power management circuitry (Ramadass and Chandrakasan, 2009).

Today, energy harvesting sources ranging from solar, wind, thermal, ambient vibration and tidal wave to salinity gradient is already available whether in consumer products or under the microscope. The efficient reuse of waste energy which gave birth to a novel Thermoelectric Power Generator (TEG) in

automobiles that scavenge energy from exhaust heat in 1998 by Nissan also gained sound attention (Ikoma *et al*., 1998). Recognizing this need, various energy harvesting technologies, different topologies and many types of power electronic interfaces for stand-alone utilization or grid connection of energy harvesting application has surfaced (Khaligh and Onar, 2009). Some of these were developed into board level or meso-scale energy harvesting systems and later followed by CMOS process implementation (Ramadass and Chandrakasan, 2009).

Energy converter topologies were developed based on a two-port power-pole building block (Mohan *et al*., 2003). Various energy conversion schemes using this power-pole were developed. The review in (Szarka *et al*., 2012) provides a summary of power converters focusing on low-power systems (<10 mW) with specific emphasis on kinetic energy harvesting systems. However, these power converters are targeted at specific individual energy harvesters. Multiple converter topologies combined these individual converter topologies while introducing certain advantages and optimizations, primarily in the combined amount of harvested power. A single shared inductor with switch matrix is used in (Bandyopadhyay and Chandrakasan, 2012) by time-division multiplexing the usage of the inverter for multiple converters. This significantly reduces the size and cost of the system with less number of costly and large inductors. A similar time-sharing method of the inductor is also employed by (Shi *et al*., 2011) with automatic digital control of switches to deliver maximum power. The Multi-Harvesting Power Chip (MHPC) of (Colomer-Farrarons *et al*., 2011) was designed to be able to collect energy from solar, mechanical vibration, heat and RF sources. Each power source used its own energy conditioning circuit.

A general block diagram of the universal power management Integrated Circuit (IC) for small-scale energy harvesting is shown in Fig. 1 and developed in (Kong *et al*., 2011) which uses dynamic resistive matching to extract maximum power from a wide input DC voltage, different energy sources and varying environmental conditions. The multiple-input boost converter in (Shi *et al*., 2011) showed that approximate matching from simplified resistor emulation is effective for near-maximum power extraction (>95%). These can be viewed as variations of possible UPC implementations if UPCs are broadly defined as energy converters which are able to accept energy from a wide range of voltages. However, the wide range of voltages will need to include very low voltages as well e.g., 20 mV for TEGs (Ramadass and Chandrakasan, 2009) which was not available in (Kong *et al*., 2011). This low-voltage startup was assisted by vibrations in (Ramadass and Chandrakasan, 2009) for bodily worn devices. As a more space-efficient alternative to mechanical assistance, a RF kick-start scheme was employed where a short RF burst wirelessly charges a storage capacitor which turns on a boost converter (Zhang *et al*., 2013). On another note, UPCs will also need to be able to process both AC and DC inputs. Most existing power conditioners require separate inputs for AC and DC sources (Bandyopadhyay and Chandrakasan, 2012; Colomer-Farrarons *et al*., 2011; Sern Mi *et al*., 2013).

The literature shows extensive research and profound interest in energy harvesting. However, there is still a lack of a low cost universal solution to battery or fossil power replacement as implementation of technology is application dependent, thereby one size does not suit all needs. Also, there is the concern of alternative energy efficiency, where in the case of a low cost crystalline silicon solar cell module, the efficiency is barely 20%. This is where advanced circuit technology comes in by introducing high efficiency, almost lossless rectifications, power boosting circuitries and timing controls. Table 1 summarizes the energy harvesting opportunities and its demonstrated capabilities of several energy sources (Bandyopadhyay and Chandrakasan, 2012).

In a nutshell, the limitations in terms of cost, efficiency, universality of harvesters and application dependency motivates this study. The future harvester should be low-cost, non-intermittent, universal in application, self-sustainable, multi-ambient input-capable and has a reconfigurable output voltage with cascadable architecture.

Table 2 shows a comparison of the UPC with previously published works having similar functionality. The UPC provides universality of input and hence reliability due to not requiring extra components. A large input voltage range and adjustable output voltage allows for flexibility in powering ULP loads.

Power management ICs developed in (Bandyopadhyay and Chandrakasan, 2012; Colomer-Farrarons *et al*., 2011; Kong *et al*., 2011; Zhang *et al*., 2013; Kim and Rincon-Mora, 2014) were fabricated and the die microphotograph for the power management IC in (Bandyopadhyay and Chandrakasan, 2012) is shown in Fig. 2 highlighting the areas used for switch matrix and drivers, control circuits, delays, pattern generator, comparators, reference and voltage divider. The architecture of power management here is similar to the proposed work in which both AC and DC sources of energy can be processed with maximum energy extraction and capability for charging external storage elements. The IC was implemented in a 0.35 μm CMOS process technology with the die occupying an area of 25 mm^2. Energy harvesters tested on the system were SANYO photovoltaic cells, MIDE piezoelectric transducers and Tellurex thermoelectric transducers with super-capacitors and 3.3 V lithium batteries for energy storage (Bandyopadhyay and

Chandraksan, 2012). The proposed power management system is able to accept a wide range of input voltages (20 mV to 5 V) and provide a fixed regulated output of 1.8 V. Power converter efficiencies are 58, 83 and 79% for thermal boost, photovoltaic boost and piezoelectric buck-boost respectively.

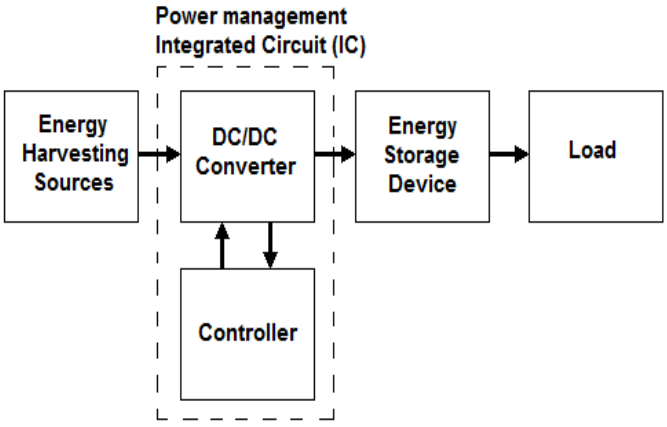

Fig. 1. General block diagram of the universal power management IC (Kong *et al*., 2011)

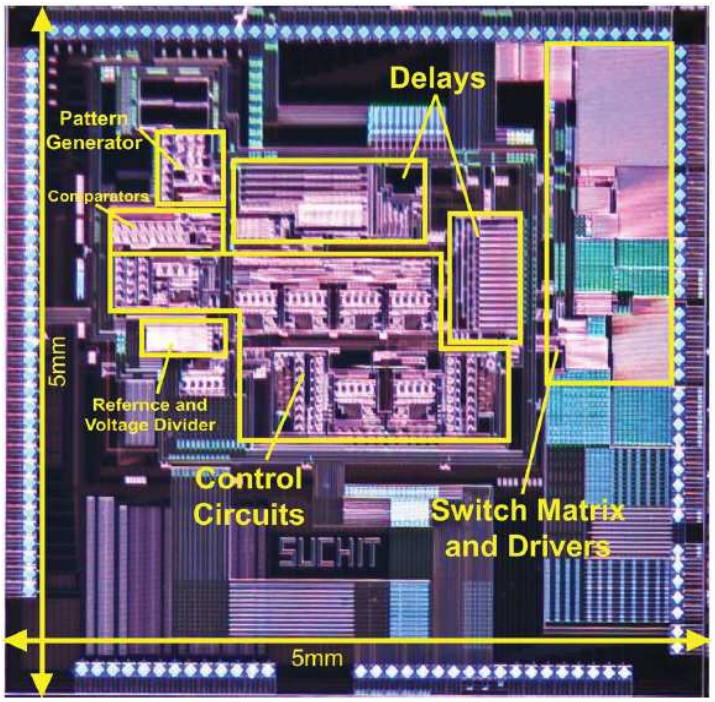

Fig. 2. Die microphotograph for the dual-path architecture in (Bandyopadhyay and Chandrakasan, 2012)

Table 1. Energy-harvesting opportunities and capabilities for various sources (Bandyopadhyay and Chandrakasan, 2012)

	Harvester types		
Parameters	Thermal	Solar	Vibration
Material, size, conditions	BiTe, 50 cm^2 ΔT~2-5 K	Si (1-2 series) 500-2000 lux	PZT (1-2 parallel) >1 g
Harvester voltage (open circuit)	50-300 mV	200-900 mV	3-10 V
Impedance value	5-10 Ω	0.05-2 kΩ	10-150 kΩ
Maximum power extraction	One time setting	Tracking	One time setting

Table 2. Energy-harvesting opportunities and capabilities for various sources

	Parameters								
Authors (Year)	Energy source	Input DC voltage	Architecture	Output DC voltage	Maximum output power	Peak efficiency	Power consumption	Process technology	Application
Colomer-Farrarons *et al.* (2011)	Photovoltaic, Vibration and RF (Magnetic Induction)	up to 2.5 V RF, 1.3-2.5 V Solar, 1-2.5 V Piezoelectric	Multi-harvesting, each source uses own energy conditioning Circuit	1.2 V RF 1.2 V Solar, 1 - 2.5 V Piezoelectric, 1.2 V Storage device	6.4 mW	55-85%	160 µW	ASIC 0.35 µm	Low power loads (e.g. sensors, interface, µP's, wireless devices etc.)
Tan and Panda (2011)	Photovoltaic and Thermoelectric	~ 3.6 V	Parallel HEH, energy sources are connected directly, uses single power converter	~ 5.5 V	621 µW	~90 %	135 µW	Hardware prototype	Wireless sensor nodes
Kong *et al.* (2011)	Any DC source	NA (tested at 5 V)	Non-inverting buck-boost Converter	NA (tested at 3 V)	NA	NA	1.23 mW	CMOS 0.18 µm	Battery-powered devices (e.g., mobile devices and wireless sensor nodes)
Bandyopadhyay and Chandrakasan (2012)	Photovoltaic, Thermoelectric and Vibration	20 mV-0.16 V Thermal, 0.15-0.75 V Solar, 1.5-5 V Piezoelectric	*Dual-path* from harvester to charger and load, multiple power converters in parallel for maximum power extraction stage	~ 1.88 V	1.3 mW Thermal Boost, 2.5 mW Photovoltaic (5-10 mW with increased switching frequency), 200 µW Piezoelectric	58% Thermal Boost, 83% Photovoltaic Boost, 79% Piezoelectric Buck-Boost	NA	CMOS 0.35 µm	DSP/µ-Controller and sensor circuits
Zhang *et al*. (2013)	Thermoelectric and/or RF	30 mV Thermal, RF (NA)	Boost converter, linear and switched-capacitor regulator	0.5 V, 1.0 V, 1.2 V, 0.25-1.0 V (50 mV steps)	~ 400 µW	38%	NA	CMOS 0.13 µm	Body sensor node SoC
Kim and Rincon-Mora (2014)	Fuel cell and Li-ion battery	1.1-1.3 V Fuel cell, 1.8 V Li-ion battery	Single-Inductor Dual-Input Dual-Output Buck-Boost	0.8 V	10 mW	70% efficiency at 0.1 mW, 83% peak	NA	CMOS 0.18 µm	Micro-sensors, biomedical implants, portable devices
This work (2015)	Any AC or DC source	20 mV-5 V	Universal source converter	0.5-5 V	>1 mW	>90%	< 100 µW	CMOS 0.13 µm	wireless sensor nodes

Statement of Problem

The main purpose of this study is to minimize the multiple converter topologies required for extracting maximum power from different types of energy harvester. Examples of multiple converter topologies are the dual-path architecture (Bandyopadhyay and Chandrakasan, 2012), the MHPC (Colomer-Farrarons *et al.*, 2011) etc. Past researchers either used optimized individual source specific converters or a combination of multiple converters to convert harvested energy into useful voltage levels. Multiple converter architectures or Hybrid Energy Harvesters (HEHs) that combine input energy from multiple sources are discussed in literatures (Ramadass and Chandrakasan, 2011; Colomer-Farrarons *et al.*, 2011; Tan and Panda, 2011). These literatures either utilize separate power management units or a single multi-harvester architecture where specific sources must be fed to corresponding converters as shown in Fig. 3.

The disadvantage of the conventional architecture is a larger number of components are required due to the multiple converters used. In its simplest form, a minimal number of two converter types are required for DC to DC conversion and AC to DC conversion respectively. A multiple-input boost converter discussed in (Shi *et al.*, 2011) is limited to DC sources in the absence of an AC to DC converter. Furthermore, the output to the load is regulated at a fixed voltage, hence not adjustable to cater to different load voltages. Therefore, this study proposes a UPC architecture which is able to detect the arbitrary inputs (e.g., photovoltaic, thermoelectric, electromagnetic, piezoelectric) before feeding the source into the universal source converter, generate an adjustable output voltage within a specific range (e.g., 0.5-5 V) and uses a hybrid storage system for improving long term storage. This reduces the need for multiple converters and the requirement to connect specific energy sources to the corresponding converters. The result is an overall reduction of the form factor of the entire power management architecture. A hybrid storage system of multiple sets of super-capacitor and Li-ion battery pairs allows for a more optimized approach to charging and discharging, allowing for an extended lifetime of the storage system.

Description (Proposed Block)

Figure 4 illustrates the proposed UPC architecture which consists of nine blocks (i.e., Block 1 to Block 9) which represents the arbitrary input sources, source limiter/ kick-start block, DC/DC Boost Converter, Storage

Block, Buck Regulator, Battery Control Block and finally the feedback control respectively. The following paragraphs will describe each of these blocks in detail:

Firstly, the Arbitrary Input Source (Block 1) may consist of any type of arbitrary inputs such as piezoelectric element, electromagnetic generator, thermal generator or photovoltaic cell. These meso-scale transducers are chosen for being commonly available commercially (Harb, 2011) to convert vibration, heat or light source to useful energy. This proposed UPC architecture is universal in the sense that it has a wide range of acceptable input voltages capable of capturing energy from any of the aforementioned arbitrary harvesters using the same I/O port. This is made possible as any one of these arbitrary sources can be fed into the Source Detector Block (Block 2) which will then detect the type of source it has received. This block determines the type of harvester by differentiating between alternating current sources from the direct current sources such as the electromagnetic generators and thermoelectric generators respectively. A zero current crossing detector to indicate existence of an alternating source as is suggested by (Kim and Kim, 2012) for their boost converter can be modified for this purpose.

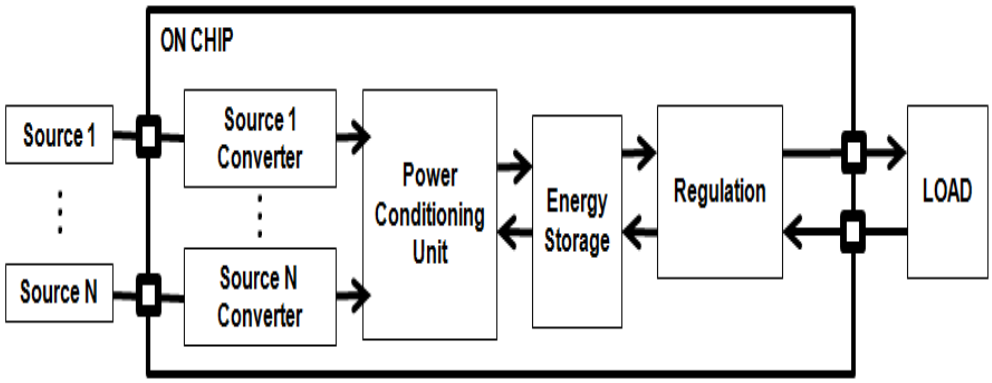

Fig. 3. Conventional architecture of HEH sources with multiple converter topologies (Bandyopadhyay and Chandrakasan, 2012; Colomer-Farrarons *et al*., 2011; Tan and Panda, 2011)

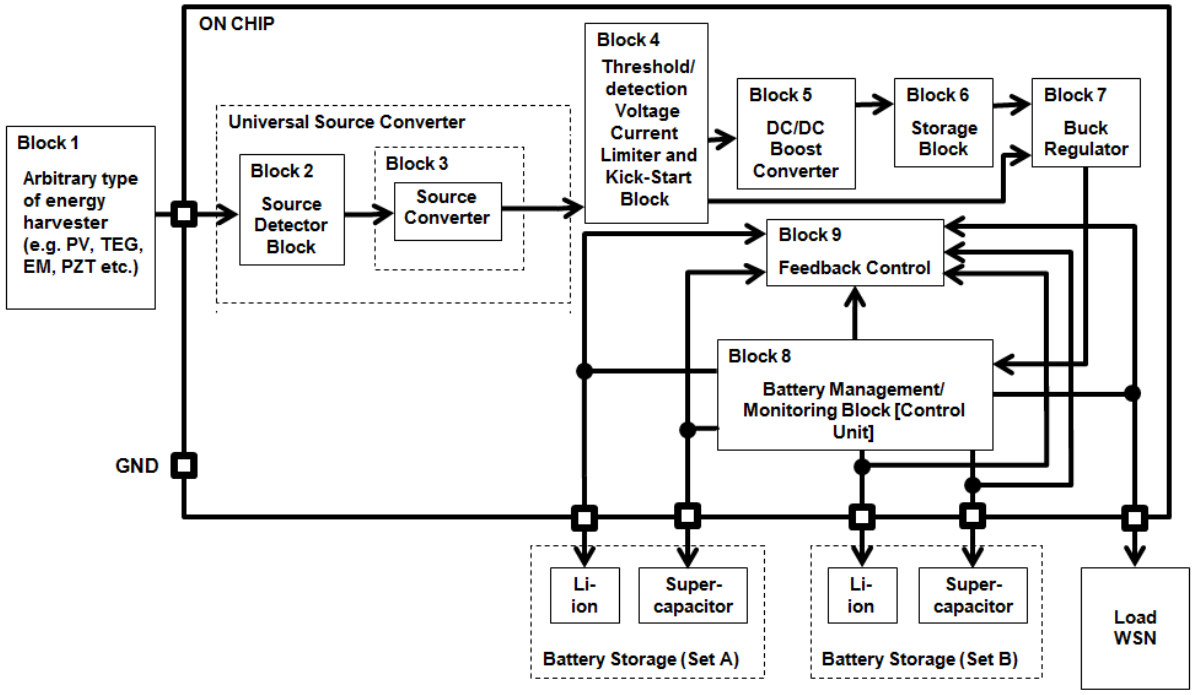

Fig. 4. Proposed block of the UPC architecture for wireless sensor network nodes

Once the harvester type is determined based on its AC or DC characteristics, the source detector control block will then feed these source voltages into the source converter block (Block 3) wherein rectification will only be activated if an AC source is detected. The rectification scheme to be used here may range from passive rectification (Hart, 2011) of full-wave cross-coupled rectification (Szarka *et al.*, 2012) to active rectification methods such as the self-start enabled synchronous rectifier (Szarka *et al.*, 2012) or voltage doublers (Bandyopadhyay and Chandrakasan, 2012; Ramadass and Chandrakasan, 2009). The latter provides higher system efficiency as compared to its full wave counterpart due to one less diode voltage drop per time and the maximum extractable power can be extracted at an elevated voltage level and a reduced current level (Szarka *et al.*, 2012). This is an advantage especially in ULP architectures as such where reduction of conduction losses is imminent. The rectified DC signals will then be passed to the next threshold detection block.

The threshold detection block (Block 4) compares the possible upper and lower limits of the rectified DC signal from the harvesters to internal reference voltages within this block. The lower limit represents a minimum threshold (~20 mV) to decide whether or not an activation of the kick start circuit (Sang *et al.*, 2012; Szarka *et al.*, 2013) is necessary while the upper limit (>~5 V) channels the access voltage either to an overvoltage protection circuit or is recycled and used for charging backup storage capacitors. The kick start circuit will be required to lift or multiply voltages (Szarka *et al.*, 2013; 2014) up to ~100 mV before the next stage of energy processing is possible. Once the voltage from threshold detection block is lifted to ~100 mV, this voltage will be passed on to be either directly regulated at the output if harvester input reaches a voltage value of >~1.5 V or further processed by the DC-DC boost converter as motivated by (Bandyopadhyay and Chandrakasan, 2012) for their parallel power transfer network.

The DC-DC boost converter block (Block 5) increases the input voltage level to a higher output level as is implemented by past literatures in their single source (Ramadass and Chandrakasan, 2009; Kim and Kim, 2012; Yu *et al.*, 2011) or hybrid source (Bandyopadhyay and Chandrakasan, 2012; Tan and Panda, 2011; Lim *et al.*, 2014) architectures. The boost topology is normally designed to operate in Discontinuous Current Mode (DCM) when reduced conduction losses (Hart, 2011; Luo and Ye, 2010) is important. Normally, resistance emulation (Shi *et al.*, 2011; Ramadass and Chandrakasan, 2011) at the input of these converters is required to ensure impedance matching between the converter and the harvester voltages and therefore maximum extracted power. A few maximum power extraction techniques have been suggested for architectures with hybrid sources such as time multiplexing (Bandyopadhyay and Chandrakasan, 2012) and pulse counting (Shi *et al.*, 2011). Here, the proposed boost converter needs to adapt to a wide range of possible impedances (Harb, 2011; CUI, 2012; SANYO, 2008; MIDE, 2013; Lim *et al.*, 2014) from the different harvesters as motivated by (Bandyopadhyay and Chandrakasan, 2012; Tan, 2013). Once maximum power is located, voltage is boosted and will enter the next energy storage block. The energy storage block (Block 6) comprises of an intermediate storage super capacitor. This temporary storage block will buffer voltages between source and load to avoid charging or harvesting intermittencies. The voltage at this point is fed into the Buck Regulator (Block 7) as it needs to be regulated before usage by the Wireless Sensor Network (WSN) node.

Next, the regulated voltage level will be fed into the battery management block (Block 8) in which it will serve as a control to power the WSN load of various voltage levels and at the same time charge the battery storage sets A and B alternatively. The battery sets are made up of the super-capacitor and Li-ion batteries (Ongaro *et al.*, 2012; Valle *et al.*, 2011). According to (Ongaro *et al.*, 2012), these two external storage type complements each other during charging in terms of energy density and charge cycle. Finally, a feedback control (Block 9) is inserted to ensure there is an adaptive control and switching between hybrid battery storage sets, load and end of charge cycles (Valle *et al.*, 2011) to ensure efficient charging and harvesting efficiencies as well as prolonging the lifespan of the battery pack.

In essence, this proposed UPC has a universal input port to support any arbitrary harvester and detects the type before relevant energy processing is done. The UPC is also capable of charging two battery storage sets and powering WSN at a wide range of output levels. The challenge is to extract maximum power regardless of input harvester, kick start at low voltage levels and directly power the output and store excess of voltages if a suitable voltage level is detected. Thus, once all of these nine blocks are integrated in the 0.13 μm CMOS technology, the expected results is a wide range of acceptable input voltage from ~20 mV to 5 V and a wide range of output voltage levels of 0.5-5 V. The expected power consumption is <100 μW and maximum output power is >1 mW (Tan and Panda, 2011) to support the WSN load and charging of the battery sets while the efficiency of >90% is expected as motivated by (Valle *et al.*, 2011).

Implementation Process of UPC Architecture (Method)

The design flow chart of the proposed UPC architecture is shown in Fig. 5 where it will begin with literature review and end with tape-out ready GDSII format. The following paragraph will describe sequentially each of the process flow in detail.

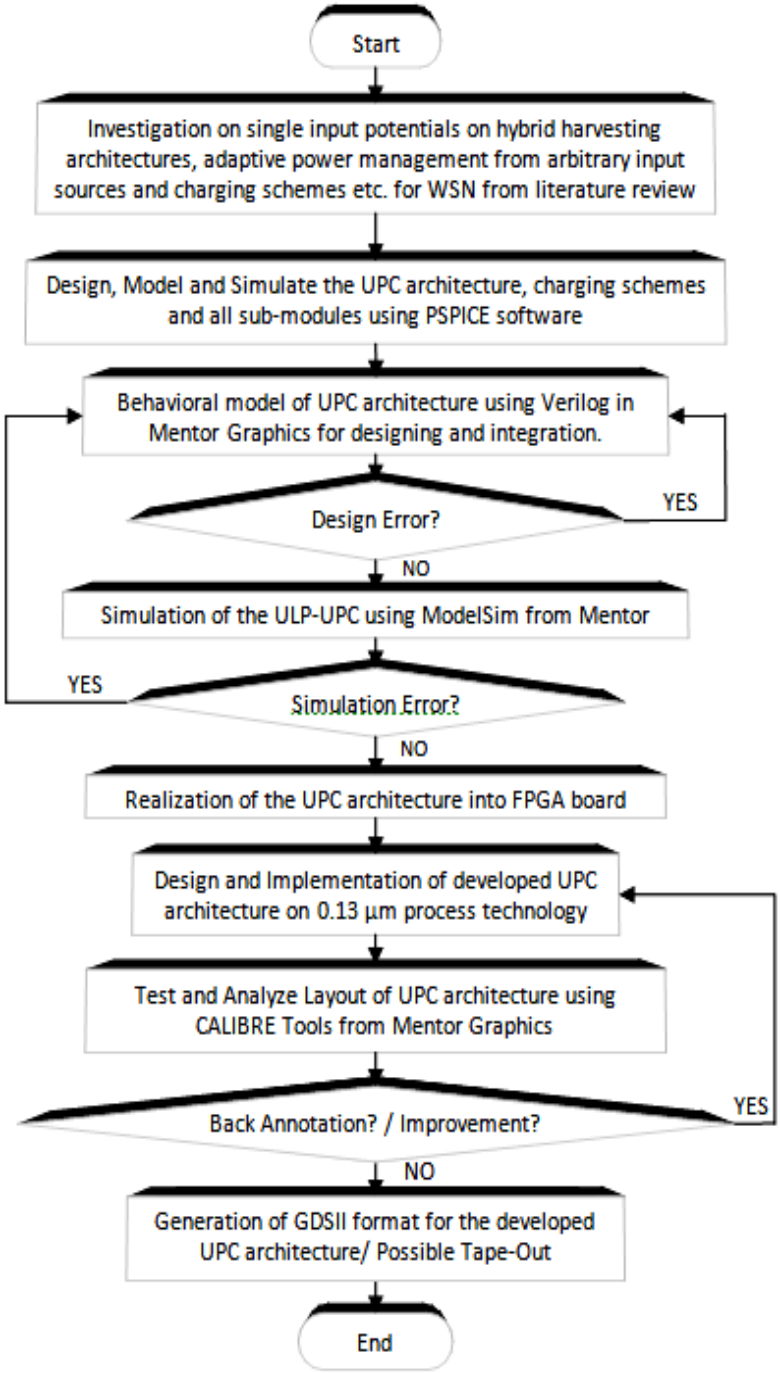

Fig. 5. Design Flow Chart of Universal Power Conditioner (UPC) Architecture

First and foremost, an extensive literature review is conducted on single input potentials on hybrid harvesting architectures, adaptive power management from arbitrary input sources and charging schemes etc. particularly for WSN. Next the UPC architecture, together with its charging schemes and all sub-modules will be modeled, designed and simulated using the PSPICE software. Once a satisfactory result is obtained, a behavioral model of the proposed UPC architecture will then be written in Verilog HDL and later simulated using Modelsim from Mentor Graphics environment. At this stage, any simulation errors will be propagated back to behavioral modeling of the UPC. Otherwise, the proposed UPC will be realized on an FPGA board. Subsequently, the developed UPC architecture will be designed and implemented as transistor level schematic

and layout drawing in the Design Architect (DA) and IC Station of Mentor Graphics environment. The proposed architecture will be implemented on a 0.13 µm process technology where the CALIBRE tools from Mentor Graphics will perform three important tests: Design Rule Check (DRC), Layout Versus Schematic (LVS) and Parasitic Extraction (PEX). Once the entire architecture is tested and analyzed, post layout simulation will be conducted and determined whether any improvement or back annotation is necessary before finally generating a tape-out ready GDSII format UPC architecture for arbitrary sources in WSN applications.

Conclusion

A UPC architecture with the ability to accept energy from any arbitrary energy harvesting source is proposed. This solution is an improvement from the separate multi-source harvesters whereby it adaptively detects the type of input source and configures appropriate charge/ harvesting levels for the WSN loads or its dual battery storage. The UPC architecture is made up of a novel universal source detector block, threshold/ current limiter block, a boost converter, buck regulator and a battery monitoring unit. The proposed architecture will power the WSN load and at the same time charge battery storage sets A and B alternatively to achieve better efficiency and longer battery life-time. This UPC architecture will be modeled, designed and simulated in PSPICE and later the behavioral model written in Verilog will be simulated in ModelSim and downloaded into the FPGA board. The entire UPC architecture will be finally implemented, tested and analyzed on 0.13 µm CMOS process technology layout in Mentor Graphics environment. The expected result of the UPC architecture is the ability to at least differentiate between 2-3 arbitrary sources and provide enough power (>1 mW) to charge external storage battery sets while powering WSN nodes which are typically in the 100 µW ranges. The power converters are expected to consume <100 µW at >90% peak efficiency with a wide input dc voltage range (20 mV -5 V). With its adjustable output voltage (0.5 to 5 V), the UPC may be utilized to power a wide range of suitable commercial or custom low-power electronic devices (e.g., wearable devices, sensors, wireless sensor nodes etc.) or charge hybrid battery sets.

Acknowledgement

The authors thank UKM for supporting this research.

Author's Contributions

Yeo Kim Heng: Conducted critical review of energy converter topologies, analysis, problem identification and writing of the manuscript.

Md. Shabiul Islam: Designed the research plan, organized and led the research, participated in analysis and problem identification, contributed to the reviewing of the article critically.

Susthitha Menon, Sawal Hamid Md. Ali and Shafii Abdul Wahab: Contributed in the entire development process of the conceptual framework, discussion and development of proposed design, drafting and review of the article.

Ethics

The authors have no conflicts of interest in the development and publication of current research.

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