American Journal of Applied Sciences

Review Articles

Architecture of Ultra Low Power Micro Energy Harvester Using RF Signal for Health Care Monitoring System: A Review

Farah Fatin Zulkifli, Jahariah Sampe, Muhammad Shabiul Islam and Mohd Ambri Mohamed

Institute of Microengineering and Nanoelectronics (IMEN),
Universiti Kebangsaan Malaysia (UKM), 43600 Bangi Selangor, Malaysia

Article history
Received: 23-01-2015
Revised: 24-04-2015
Accepted: 02-07-2015

Corresponding Author:
Farah Fatin Zulkifli
Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM), 43600 Bangi Selangor, Malaysia
Email: frh_fatin@yahoo.com

Abstract: This research presents architecture of Ultra Low Power (ULP) Micro Energy Harvester (MEH) using Radio Frequency (RF) signal as an input. RF has many advantages compared to other ambient sources because it is not affected by changes of weather or time, does not require heat or wind exposure and it can be moved randomly within the bound of the transmission source. When RF is used as the sole input, the designer needs to consider impedance matching as the most important element so that the antenna can transfer maximum power. The existing energy harvesters apply conjugate matching network as the current solution. However, this method causes some difficulties since the solution requires consideration of both voltage boosting and conjugate matching network simultaneously. To solve this problem, we propose ULP Radio Frequency Micro Energy Harvester (RFMEH) that will utilize a control loop as voltage boosting adjuster and network tuner to achieve maximum power transfer and minimum power reflection. The proposed architecture will also improve the RF-DC conversion efficiency and the sensitivity of the system. This is achieved using an efficient rectification scheme to convert RF to DC, DC-DC boost converter to increase the dc output voltage, adaptive control circuit to adjust the switching timing of boost converter, voltage limiter and regulator to produce the best output voltage. The proposed ULP RFMEH architecture will be designed and simulated using PSPICE software, Verilog coding using Mentor Graphics and functional verification using FPGA board (FPGA) before being implemented in CMOS 0.13 µm process technology. The proposed architecture will deliver approximately 2.45 V of output voltage from low input power level (-20 dBm) with an efficiency of more than 60%. This design will minimize the power consumption as compared to previous achievements and it can be applied in supplying power for health care monitoring systems or micro biomedical applications.

Keywords: Radio Frequency Micro Energy Harvester (RFMEH), Ultra Low Power (ULP), Impedance Matching, Health Care Monitoring System

Introduction

In recent years, there is an increasing request for energy harvesting system that can provide input power to ULP sensor and wireless device. Conventionally, electrochemical batteries were used as a source for powering each sensor node. However, battery is large, expensive and unfeasible to be replaced frequently especially in rural areas. There are many energy sources surrounding us such as thermal, RF, photovoltaic and mechanical sources like wind and vibration (Devi *et al*., 2012). The potential of energy harvester to absorb power and fill up the energy storage when necessary can reduce maintenance cost or prolong battery life. Small electromechanical devices which capture, harvest and convert the ambient energy into electrical energy are known as Micro Energy Harvesters (Sarker *et al*., 2011).

Nowadays, researchers have developed energy harvesters to power wireless sensor nodes as self-powered to create many innovative applications such as medical monitoring, machining-condition monitoring and structural-health monitoring (Chung *et al*., 2014). Most of the implanted biomedical devices are passively utilizing RF signals as the power provider to extend

battery life and to prevent any chemical hazards due to battery usages (Le *et al*., 2008). Additionally, for most ULP devices which require low maintenance, long lifespan, small size and light weight, removing the battery is recommended. To reduce the power consumption circuit in the future, one solution is to build a self-powered system which can utilize ambient energy from the environment for maintaining circuit operation. This method potentially cut down the cost needed for regular battery replacement. Moreover, in some applications, depending on the sensor location, battery replacement may be both uneconomical and unpractical, or may endanger human life.

The vision of realizing an autonomous Wireless Sensor Network (WSN) attracted much attention recently as it offers a wide range of applications (Nintanavongsa *et al*., 2012). These WSNs can sense, process and wirelessly transmit information such as temperature, humidity, location and sensor identification. Typical applications are inventory management, smart buildings, structural maintenance and health monitoring in personal Body Area Networks (BANs) (Stoopman *et al*., 2014). Also, there are some applications like implantable Bio Medical Sensors, in which replacing batteries from time to time is not feasible (Shrivastava *et al.*, 2013). The usage of wired charging system limits the movement of the patient which is sometimes necessary for the quick recovery of the patient and also the wire does require an incision through the human tissue which can lead to infections. The field sensors can be powered by running cables to each sensor units, but the use of power cables in hazardous environment may lead to mishaps and therefore must be replaced with a safer option.

Related Research

Energy Harvesting which was inspired from the windmill and water wheel is an operation of absorbing energy from the ambient sources and converting it into useful electrical energy (Chalasani and Conrad, 2008). Demands on WSNs and Radio Frequency Identification (RFID) has increased the importance of power supply generation for these types of circuits (Shokrani *et al*., 2014). The usage of batteries is usually expensive, inappropriate and easily drains out due to insufficient volume of energy (Swapna Kumar and Kashwan, 2013). Therefore it is crucial to use RF energy harvesting method as a power supply. Figure 1 shows a general wireless RF power transmission system. Generally, an antenna is connected to a rectifier to form a rectenna that converts the incident RF power into usable Direct Current (DC) power that will pass through an Energy Storage System (ESS) before being delivered to the load Visser and Vuller (2013) and Dahiya *et al*. (2014) reported that power at the receiver and V_{rms} (induced voltage) are inversely proportional to the distance.

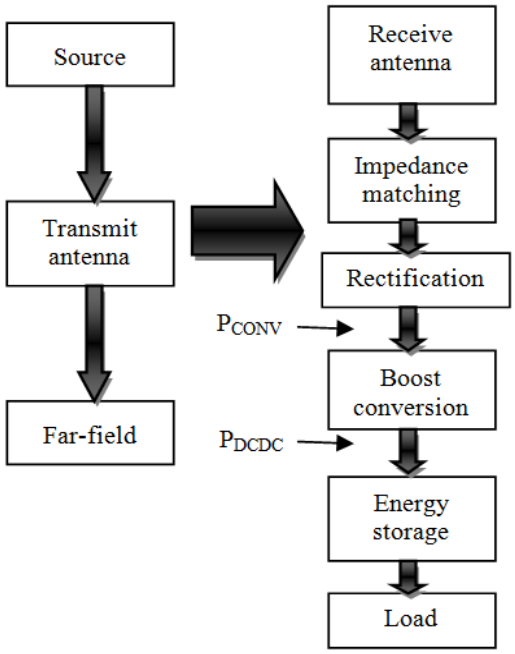

Fig. 1. Wireless RF power system (Visser and Vuller, 2013)

Basically, the design of RF Micro Energy Harvester consists of an antenna with impedance matching circuitry, rectifier, power conversion and energy storage module. The overall energy harvester efficiency, η is given by Equation 1:

$$\eta = \left(P_{DC}\right) / \left(P_{(RF-IN)}\right) = \eta_{Ant}\, \eta_{matching}\, \eta_{rec} \quad (1)$$

where, η_{Ant}, $\eta_{matching}$ and η_{rec} are efficiency of antenna, impedance matching and combination of rectifier, DC power converter with energy storage, respectively. The key factors that lead to RF harvester optimization are the sensitivity and efficiency. High sensitivity should be considered so that it can harvest from ultra-low levels of RF energy while high efficiency is the ability to minimize losses by converting maximum energy into useful electrical output (Park *et al.*, 2008). There are many ambient RF power sources available in urban areas as illustrated in Fig. 2 (Shiho, 2011).

The RF energy harvester implementations are either directly used as ULP devices power supply or as energy storage for necessary use only. Devi *et al*. (2012) used a 900 MHz system with a Villard voltage doubler circuit which produced an output voltage of 2.12 and 5 V through simulation and measurement respectively at input power level of 0 dBm. Papotto *et al*. (2011) disclosed that an output voltage of 1V can be obtained from an input power as low as -24 dBm (4 μW) at 915 Mhz. Mansano *et al*. (2013) produced 1.35 V into 1 MΩ load for an input -18.2 dBm through simulation.

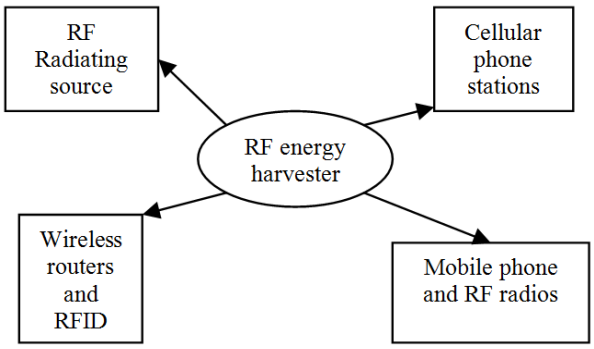

Fig. 2. Radio wave energy sources in urban areas (Shiho, 2011)

Hong *et al*. (2013) used a seven stage Cockroft-Walton voltage multiplier, achieved 2 V output voltage with -9 dBm (0.13 mW) sensitivity at an operating frequency of 2.48 GHz. Arrawatia *et al*. (2012) works on a new differential microstrip antenna, off chip matching circuit, on chip novel CMOS rectifier and control circuitry in 180nm CMOS technology which leads to 40% efficiency for -11 dBm received power. Ping-Hsuan and Tao (2013) designed a 900 MHz system which implemented an adaptive control and startup circuit that produced 2 V output voltage at input power of -15 dBm. Stoopman *et al*. (2014) used 5 stages cross connected differential rectifier with a 7 bit binary weighted capacitor bank demonstrate a -27 dBm sensitivity for 1V output across a capacitive load. Meanwhile, Sivaramakrishnan and Jegadishkumar (2011) modified simple voltage doubler circuit to use for charging mobile phones for average input power 20 dBm.

The efficiency of an antenna is mainly determined by antenna impedance and converter circuit impedance. Match impedance occurs when impedance of the antenna is the complex conjugate of the circuit impedance (Devi *et al.*, 2012). Ping-Hsuan and Tao (2013) implemented off-chip inductors (Q >80) for maximum power transfer from the source. Shokrani *et al.* (2014) have carried out two strategies where the first approach is to use off-chip inductors as there is no limitation for their inductance value while the second approach is to use on-chip inductors. They found out that using off chip inductors improves the sensitivity of the rectifier significantly (-18 dBm), while using the on chip inductor reduces the rectifier's efficiency. Arrawatia *et al*. (2012) implemented an approach to calculate the input impedance of the rectifier which is called as Periodic Steady State (PSS). Papotto *et al*. (2011) stated that power losses can possibly be ignored as long as high-Q component is implemented. However, co-design need to be considered to balance losses and reflection if only low Q matching element available. Meanwhile, Dias *et al.* (2014) introduced a source pull mechanism in order to obtain optimum input source load to maximize the efficiency. Taris *et al*. (2012) and Lenin and Abarna (2014) employed a Smith chart matching method to design the matching circuit with the help of software.

In designing the optimized CMOS rectifier, the structure of the diode and its characteristics such as forward bias current, threshold voltage and leakage current play critical roles in the performance of the rectifier circuit. Higher DC voltage can be achieved when low threshold rectifying device (diode or MOSFETs) in multiple stages are employed but too many stages may degrade the efficiencies due to accumulated parasitic capacitances at high frequency (Roscoe and Judd, 2013). Bo and Goldsman (2013) discussed a design procedure to find optimal size of MOSFETs connected diode. Shokrani *et al.* (2014) and Shrivastava *et al.* (2013) introduced a new structure of diode connected transistor which is the bulk is connected to the drain instead of the source to reduce the reverse current of the diode. Theilmann *et al*. (2012) have combined a cross-connected and diode bridge rectifier to design a µW complementary bridge rectifier in order to prevent overflow leakage current.

In most of the cases, the input signal voltage is much smaller than the typical rectifier threshold voltage. Work by (Devi *et al*., 2012; Nishimoto *et al*., 2010; Lenin and Abarna, 2014) utilized zero bias Schottky diodes due to the low substrate losses, very fast switching, low forward voltage and non-symmetric properties that allows unidirectional flow of the current under ideal case. Bo *et al*. (2013) discussed a self-biasing technique by using the biasing resistors to provide DC bias voltage at the gate of the MOSFET connected diode to increase the charging current. In contrast to traditional Schottky and diode connected MOS transistor rectifier, Mansano *et al.* (2013) utilized an Orthogonally Switching Charge Pump Rectifier, CPR (OS-CPR) comprises of MOS transistors as voltage controlled switches with a capacity to operate in both weak and strong inversion regions. Floating gate technique, enable reducing or cancelling the threshold voltage of the MOS transistor as proposed by Le *et al*. (2008) however this technique requires a pre-charge or calibration phase and also suffer from leakages. Arrawatia *et al*. (2012) proposed a rectifier without any external bias circuit needed by arranging every alternate transistor biased using the node voltage from the next transistor. Papotto *et al*. (2011) deployed a fully passive threshold self-compensation scheme that increases the gate bias offset by extending length of the compensating bridges.

Another critical aspect to the operation of low power energy harvesting is the method of low power voltage boosting that we use to turn on the MOSFETs, especially when involved with CMOS. Bo *et al*. (2013) and Stoopman *et al.* (2014) implemented an LC resonant circuit to generate a large voltage across the MOSFET, thereby turning it on even though the input power is very low. Lim *et al*. (2014) reported on how a dc-dc boost

converter can help to increase the output voltage from as low as 18 to 907 mV in to 310 mV to 27.9 V by utilizing suitable parametric value. Wahab *et al*. (2014) also presented a simulation result showing passive component based boost converter could increase input voltage from 0.1-0.5 to 7-35 V. Shrivastava *et al*. (2013) and De Donno *et al*. (2013) implemented charge pump rectifier to boost the battery voltage.

According to Parks *et al*. (2013), two critical elements which contribute to the effectiveness of the RF harvester are the sensitivity and per-operation energy. Yakovlev *et al*. (2012) reported on their article that low available power is one of the constraints which demand the use of low power on chip circuitry. To improve power extraction, Nintanavongsa *et al*. (2012) introduced an optimal dual stage design to achieve approximately 100% improvement. Motiur Rahaman *et al*. (2015) implemented self-powered conditioning circuit which consists of voltage doubler, charge pump, dc-dc converter and bypass path with the capacitor. Jun *et al.* (2007) discussed on multiple output rectifier and a superposition method by considering the effect of conduction angle, leakage current and body effect. Table 1 summarized previous paper works on RF energy Harvester**.**

Bo *et al.* (2013), Stoopman *et al*. (2014), Ping-Hsuan and Tao (2013), Papotto *et al*. (2011) have reported on fabricated die micrographs in their paper respectively. Figure 3 shows an example of micrograph of the test chip that reported by Ping-Hsuan and Tao (2013) which is similar to the architecture that we propose in term of sub modules implementation. This design is implemented in a 0.18 µm CMOS Technology with the core area of 500×550 μm^2. From their findings, at P_{IN} equal -15 dBm, the measured end-to-end efficiency is 35.7%. The circuit consumes 5.6 µW and the output power is 11.8 µW, while at P_{IN} equal -10 dBm, PCE reached 44%. This chip shows the arrangement of rectifier, voltage detection, adaptive control circuit, passive components and reference generation sub-blocks which covered some of the main portion of the overall RF energy architecture.

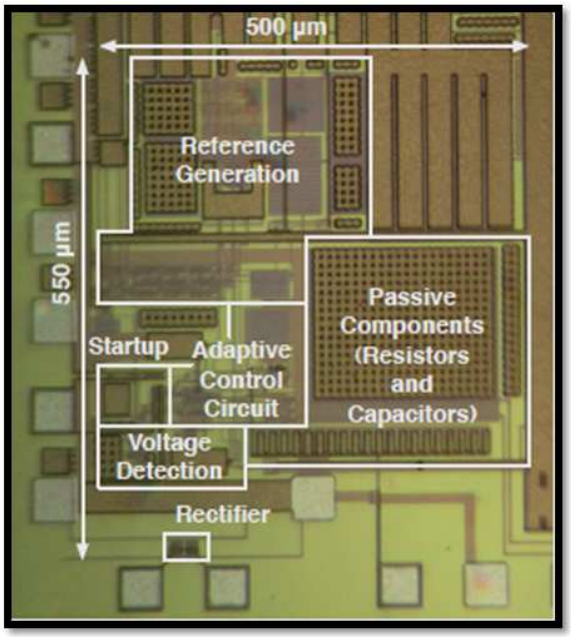

Fig. 3. Micrograph of the chip test (Ping-Hsuan and Tao, 2013)

Table 1. Summary on past researcher's work

Researcher (year)	Architecture	DC-DC boost	Control loop	Freq.[a] (MHz)	P_{IN} (dBm) /(W)	P_{OUT} (W)	V_{OUT} (V)	R_{LOAD} (Ω)	η (%)	Process tech. (nm)	App.[b]
Papotto *et al*. (2011)	17- stage self - compensated rectifier	No	No	915	-18.8 dBm (13.1 µW)	1.44 µ	1.2	1 M	11	90	Battery-less equipment
Shrivastava *et al.* (2013)	3-stage voltage multiplier, link monitoring	Yes (multi-phase voltage doubler charge pump,)	No	Not stated	-9 dBm (0.125 mW)	0.9 µ	30×10^{-3}	1 K	0.71	Not stated	Charge batteries
Bo *et al*. (2013)	Voltage doubler with boosting circuit and pre-set biasing network (dual band)	Yes	No	900 1900	-19.3 dBm (11.7 µW)	1.75 µ 1.425 µ	1.448 1.12	1.2 M 0.88 M	14 11.4	130	Charge batteries
Ping-Hsuan and Tao (2013)	Adaptive control, startup circuit, differential rectifier, switched inductor boost converter, MPPT	Yes	Yes	900	-15 dBm (31.6 µW)	11.8 µ	2V	Not stated	35.7	180	RFID, WSN and biomedical implantable devices
Mansano *et al.* (2013)	5-stage passive voltage boosting and a switching charge pump rectifier	Yes (charge pump)	No	915	-18.2 dBm (15.1 µW)	1.8 µ	1.35V	1 M	11.9	90	RFID, WSN
Stoopman *et al*. (2014)	5-stage cross connected differential rectifier,7 bit weighted capacitor bank	No	Yes	868	-17 dBm (19.95 µW)	7.98 µ	1.62	0.33 M	40	90	WSN
Shokrani *et al.* (2014)	5-stage rectifier with new bulk connection, voltage limiter	No	Yes	900	-9 dBm (0.126 mW) -18 dBm (0.016 mW)	0.018 m 0.0029 m	1.1	Not stated	14.46 (on chip) 18.08 (off chip)	180	WSN and RFID
This work (2014)	Rectifier, Control loop, adaptive control circuit, regulator and voltage limiter	Yes	Yes	915	-20 dBm (0.01 mW)	6 µ	2.45	1 M	60	130	Micro power health care monitoring system

a. Frequency, b. Application

Problem Statement

The target of this research is to overcome the problem faced by many researchers in RF energy harvesters which struggling on improving their design due to low conversion ratio because of relatively low ambient input. As the receiving RF power is generally weak (less than -10 dBm for ambient RF power), the most important design consideration is to maximize the power conversion efficiency. Two conventional topologies as shown in Fig. 4 and 5 are the architecture that we have referred to improve our proposed design.

The major design constraint for long range RF harvesters is to generate a sufficiently large voltage to activate the rectifier with a few microwatts of power because CMOS transistors inherently are voltage controlled devices. Some solutions have been proposed to reduce the rectifier turn-on voltage by using (near) zero threshold voltage (V_{th}) transistor, gate pre-biasing or V_{th} self-cancellation schemes (Papotto *et al*., 2011). However the high fabrication costs, calibration phase or reverse current leakage make these solutions too expensive and impractical. Fig. 4 shows a conventional block diagram with a feedback which control voltage boosting and tuning network that compensates variation at the interface that may occur in a realistic environment. Stoopman *et al*. (2014) optimized the antenna-rectifier interface by using a low resistive and high-Q interface. Subsequently, they proposed differential rectifier with complementary MOS diode in the last rectifying stage to improve the harvester's ability to store and hold energy over a long period of time.

Ping-Hsuan and Tao (2013) achieved high Power Conversion Efficiency (PCE) on their design illustrated in Fig. 5 by implemented an efficient power path structure and low power implementation of the control circuit. In this existing design, the rectifier's PCE is optimized by adaptively adjusting the effective loading from the boost converter according to instant input power level. Basically, the harvesting technologies constraint is on the efficiencies and effectiveness of the harvesting devices. The design by Stoopman *et al*. (2014) as in Fig. 5 is improving the sensitivity, output voltage and the efficiency if compared to design by Ping-Hsuan and Tao (2013) as in Fig. 4. However, the power consumption for design in Fig. 4 is much smaller. Our proposed design will try to improve those key elements by proposing efficient impedance matching which is controlled by control loop, high efficiency rectification scheme and a boost converter which is controlled by adaptive control circuit. This proposed design is also targeting on lowering the power consumption to achieve optimal performance results. Every component will be selected based on their power consumption and also the implementation of wireless protocol. This reduction in power consumption and operating voltage is important to increase the flexibility of applications.

This study proposes a control loop to compensate any variation at the antenna-rectifier interface and maintain a resonance so that it can utilize maximum available input. Another challenge is to maintain the optimal PCE value for the rectifier, by using an adaptive control circuit to control the switching timing of DC-DC boost which is inspired by Ping-Hsuan and Tao (2013).

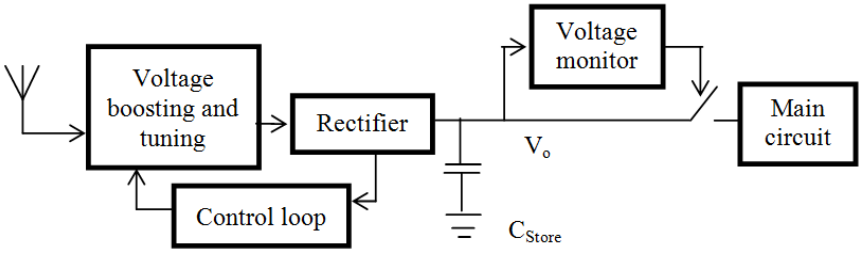

Fig. 4. Block diagram on the implementation of control loop (Stoopman *et al*., 2014)

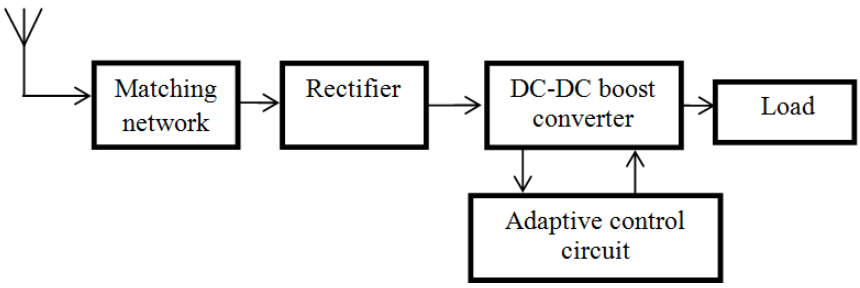

Fig. 5. Block diagram of the existing RF energy harvester with adaptive control circuit (Ping-Hsuan and Tao, 2013)

This adaptive control is open loop, as it approaches zero current with tolerable accuracy while it does not detect the inductor current. As compared to other techniques of zero current detection which using comparators or OpAmps (Kadirvel *et al*., 2012), this design occupies small area (130×130 μm^2) and it cause less power losses. Our propose architecture will be implemented on a 0.13 μm CMOS process technology to improve the efficiency and sensitivity of the existing RF energy harvester.

Description (Proposed Block)

The proposed RF energy harvester block diagram is shown in Fig. 6. It consists of eight sub-blocks which represents the antenna, voltage boosting and tuning, rectifier, control loop, adaptive control circuit, dc-dc boost converter, voltage limiter and regulator. All eight blocks will work together to increase the sensitivity and efficiency of the micro energy harvester. The explanation of each block will be subsequently described below.

Firstly, the source of this system is RF signal which can be captured from mobile phones, potentially supplying power for short-range sensing applications. Other sources such as Wi-Fi routers and wireless end devices such as laptop are also easily discovered. For short range operation, a small volume of energy can be harvested from Wi-Fi router transmitting at 50 to 100 mW. Meanwhile, for long range operation, higher gain antennas are required to harvest RF energy from broadcast radio towers and mobile base stations (Pradhan *et al*., 2014).

Secondly, antenna (block 1) is used for absorbing RF energy from the surrounding sources. A proper design of receiving antenna is crucial because the volume of harvestable energy is determined by the parameters, such as radiation pattern, gain and impedance bandwidth (Sim, 2010). Impedance of antenna and the converting circuit really contribute to the efficiency.

Thirdly, there is a voltage boosting and tuning block (block 2). Voltage boosting in this case will act much like the designed by Stoopman *et al.* (2014) which combines the inductive behavior of a high Q loop antenna with the capacitive input impedance. If resonance happens, there will be high a dc current flow across the inductor which causes voltage boosting. To obtain resonance, a parallel capacitor in the voltage boosting network can be set. However, high Q systems are very sensitive to any of input power level, environmental changes or process mismatch. Here is where we need tuning to compensate for these variations.

Once voltage is boosted, rectifier will be switched on. A rectifier (block 3) will be used to convert low input RF power to DC power. Stoopman *et al.* (2014; Ping-Hsuan and Tao, 2013) suggested the usage of differential rectifier which has its own benefit where its symmetry cancels all even order harmonic currents. In practice, this implies that it is sufficient to only suppress the 3rd harmonic in order to prevent power loss due to reradiation. In this structure, the output voltage and common-mode gate voltage generated during rectification provide additional biasing and effectively reduces the required turn-on voltage. Due to this self-cancellation, the rectifier can be activated at lower input power levels than other similar topologies. The rectifier can be any types such as full wave bridge rectifier, single shunt full wave rectifier, or other hybrid rectifiers. The diode especially used to determine the efficiency. But recently, rectifier with High Electron Mobility Transistors (HEMTs) or Field Effect Transistors (FETs) are expected to increase the efficiencies (Pradhan *et al*., 2014).

Plus, the rectifier nonlinear input impedance also varies with frequency and input power. This makes the high Q interface very sensitive to any impedance variation. To compensate for this, a control loop (block 4) is added to tune the impedance such that a resonance is created with the antenna (Stoopman *et al*., 2013). As the antenna and rectifier reactance at the interface influences both the resonance frequency and the passive voltage boost of the interface, it is decided to compensate only for reactive variations. This way, the loop still improves the RF energy harvester robustness while taking advantage of the passive voltage boost obtained from the high Q resonator.

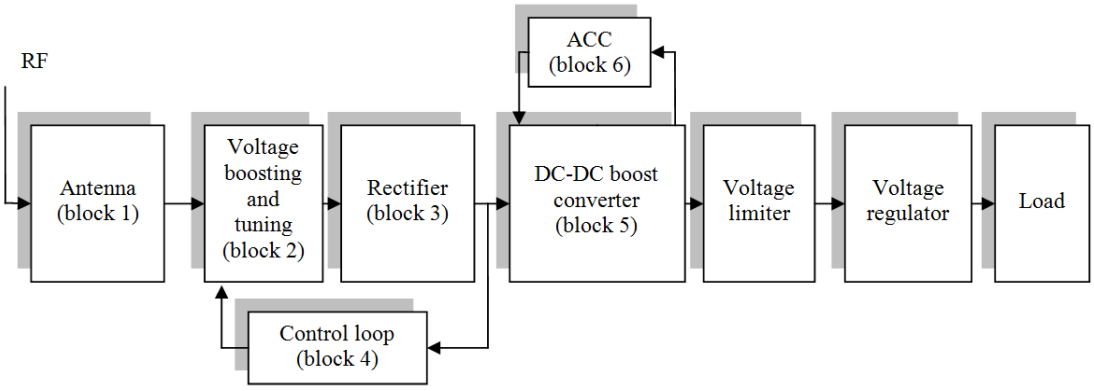

Fig. 6. Proposed block diagram of RFMEH

The DC output of the rectifier will be passed to dc-dc boost converter (block 5). This block will function as a converter with an output voltage greater than the source voltage. This booster can adjust the effective load resistance seen by the rectifier by changing its switching timing which will be controlled by adaptive control circuit. The mechanism of Adaptive Control Circuit (ACC) (block 6) is inspired by Ping-Hsuan and Tao (2013) where VDC is first compared with a reference VREF. In this design, VREF is generated from a band gap circuit. It is made adjustable to account for process variations.

Next, there is a voltage limiter (block 7) which limits the DC-DC boost's output voltage to certain level to prevent the CMOS transistor from breaking down (Ouda *et al*., 2013). The input voltage of this block is the output voltage of the boost converter. The output voltage rises up and limited by the proposed robust and powerful limiter circuit. Finally, the regulator (block 8) will control or maintain the storage voltage to a constant value to power load circuit (Shokrani *et al*., 2014).

Materials and Methods

This work will be performed by using the design-flow as illustrated in Fig. 7.

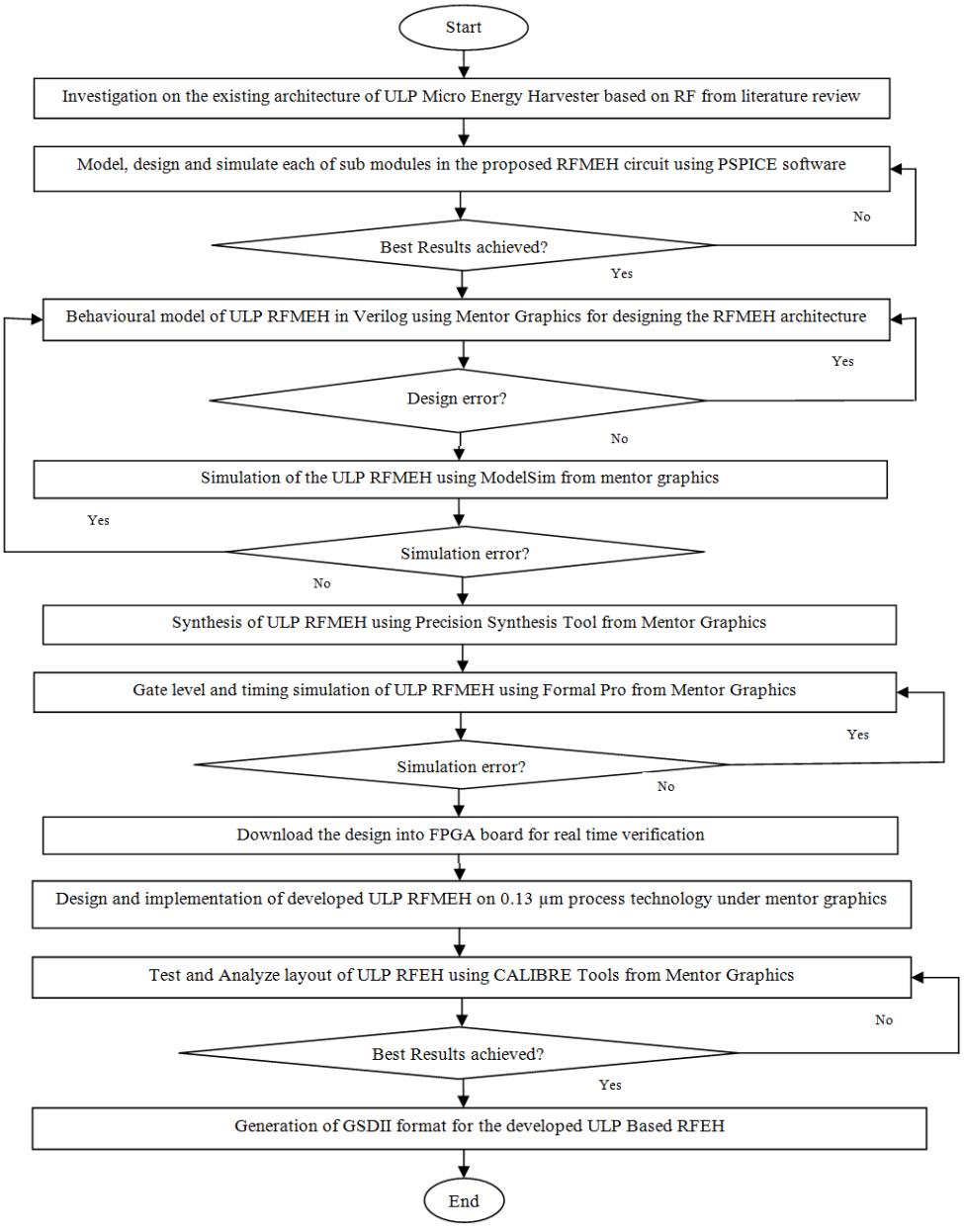

Fig. 7. Flow diagram

To perform this work, we will firstly investigate the literature background on ULP RFMEH based on previous research works. From there, a scope of project will be determined and the new ULP RFMEH architecture concept will be proposed. Then, each block of the ULP RFMEH will be modeled, designed and simulated using PSPICE Software. If the simulation results achieve the best result with no error especially in terms of efficiency, power consumption, input and output voltages, then we will proceed to the behavioral model written in Verilog using Mentor Graphics. This HDL based design of ULP RFMEH will be simulated in the ModelSim and any error in the design or simulation will lead back to redesigning stage. After that, this behavioral model will be synthesized using Precision Synthesis tool to enable a gate level simulation in the Formal Pro tool. Any error occuring in this stage will lead back to the synthesis stage. Next, this optimized ULP RFMEH design will be downloaded into the Field Programmable Gate Array (FPGA) board for functional verification. If it is successfully implemented, the ULP RFMEH circuit design will be converted into gate level model on the 0.13 µm process technology by using Mentor Graphics' Design Architecture and IC station. When the layout is ready, testing and analysis will be carried out and multiple validations will be managed by CALIBRE tool to check either any improvement is needed before the final implementation. This is important to avoid any deviation in terms of parasitic, timing or power issues. After verification on the final layout is completed, the tape-out ready GDSII format can finally be generated to possibly be fabricated for micro bio-medical applications with RF as the ambient input source.

Conclusion

The design of ULP micro energy harvester using RFMEH signal has been proposed. The main target is to maximize the extracted input and minimize the power losses obtained from Radio Frequency Micro Energy harvester. This will be achieved by using impedance matching, DC-DC boost, control loop, adaptive control circuit, voltage limiter and voltage regulator. This ULP RFMEH will be designed and simulated using PSPICE software, Verilog coding using Mentor Graphics and functional verification using FPGA board (FPGA) before being implemented in CMOS 0.13 µm process technology under Mentor Graphics and the final layout is being generated. Finally, the expected result is to achieve 60% for the efficiency and output voltage approximately 2.45 V for input level as low as -20 dBm. The result will be compared with previous conventional method. The aim of this design is to provide sufficient power for the sensor related to health monitoring system and reduce the usage of battery.

Acknowledgement

The authors would like to thank all the members of Micro and Nano Electronics System (MINES) laboratory for their assistance in the testing and anonymous reviewers for valuable comments and suggestions

Funding Information

This research supported by HICOE (AKU95) and FRGS (FRGS\2\2014\TK03\UKM\02\1) grants funded by Ministry of Education.

Author's Contributions

Farah Fatin Zulkifli: Involved in data investigation, summarizing the information and drafting the manuscript.

Jahariah Sampe: Designed the research plan and organizing the study, helping in interpretations of data and reviewing the manuscripts.

Muhammad Shabiul Islam: Assist with supervision, designed the research plan, interpretations of data and contributed to the writing and reviewing the manuscript.

Mohd Ambri bin Mohamed: Assist with supervision.

Ethics

This article is original and has not published elsewhere.

References

Arrawatia, M., V. Diddi, H. Kochar, M.S. Baghini and G. Kumar, 2012. An integrated CMOS RF energy harvester with differential microstrip antenna and on-chip charger. Proceedings of the 25th International Conference on VLSI Design, Jan. 7-11, IEEE Xplore Press, Hyderabad, pp: 209-214. DOI: 10.1109/VLSID.2012.72

Bo, L. and N. Goldsman, 2013. Voltage doubler design procedure for low ambient RF energy harvesting applications. Proceedings of the International Semiconductor Device Research Symposium, Dec. 11-13, Maryland, pp: 1-2.

Bo, L., S. Xi, N. Shahshahan, N. Goldsman and T. Salter *et al*., 2013. An antenna Co-design dual band RF energy harvester. IEEE Trans. Circuits Syst. I: Regular Papers, 60: 3256-3266. DOI: 10.1109/TCSI.2013.2264712

Chalasani, S. and J.M. Conrad, 2008. A survey of energy harvesting sources for embedded systems. Proceedins of the IEEE Southeastcon, Apr. 3-6, IEEE Xplore Press, Huntsville, pp: 442-447. DOI: 10.1109/SECON.2008.4494336

Chung, T.K., C.M. Wang, P.C. Yeh, T.W. Liu and T. Chia-Yuan *et al*., 2014. A three-axial frequency-tunable piezoelectric energy harvester using a magnetic-force configuration. IEEE Sensors J., 14: 3152-3163. DOI: 10.1109/JSEN.2014.2325675

Dahiya, R., A.K. Arora and V.R. Singh, 2014. Analysis of wireless sensor networks with energy harvesting capabilities of transmitter and receiver antenna. Int. J. Eng. Innovative Technol., 3: 120-123.

De Donno, D., L. Catarinucci and L. Tarricone, 2013. An UHF RFID energy-harvesting system enhanced by a DC-DC charge pump in silicon-on-insulator technology. IEEE Microwave Wireless Compon. Lett., 23: 315-317. DOI: 10.1109/LMWC.2013.2258002

Devi, K.K.A., N.M. Din and C.K. Chakrabarty, 2012. Optimization of the voltage doubler stages in an RF-DC convertor module for energy harvesting. Circuits Syst., 3: 216-222. DOI: 10.4236/cs.2012.33030

Dias, L.F.R., A. Boaventua and N.B. de Carvalho, 2014. RF-DC converter efficiency optimization using source-pull techniques. Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits, Apr. 2-4, IEEE Xplore Press, Leuven, pp: 1-3. DOI: 10.1109/INMMIC.2014.6815099

Hong, S.S.B., R.B. Ibrahim, M.H.M. Khir, M.A. Zakariya and A. Daud, 2013. WI-FI energy harvester for low power RFID application. Progress Electromagnetics Res. C, 40: 69-81. DOI: 10.2528/PIERC13041608

Jun, Y., K. Wing-Hung and T. Chi-ying, 2007. Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications. IEEE Trans. Circuits Syst. I: Regular Papers, 54: 153-166. DOI: 10.1109/TCSI.2006.887974

Kadirvel, K., Y. Ramadass, U. Lyles, J. Carpenter and V. Ivanov *et al*., 2012. A 330nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting. Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers, Feb. 19-23, IEEE Xplore Press, San Francisco, pp: 106-108. DOI: 10.1109/ISSCC.2012.6176896

Le, T., K. Mayaram and T. Fiez, 2008. Efficient far-field radio frequency energy harvesting for passively powered sensor networks. IEEE J. Solid-State Circuits, 43: 1287-1302. DOI: 10.1109/JSSC.2008.920318

Lenin, A. and P. Abarna, 2014. Design and simulation of energy harvesting system using GSM signal. Int. J. Latest Trends Eng. Technol., 3: 13-25.

Lim, M.S.M., S.H.M. Ali, S. Jahariah and M.S. Islam, 2014. Modelling of hybrid energy harvester with DC-DC boost converter using arbitary input sources for ultra-low-power micro-devices. Proceedings of the IEEE International Conference on Semiconductor Electronics, Aug. 27-29, IEEE Xplore Press, Kuala Lumpur, pp: 28-31. DOI: 10.1109/SMELEC.2014.6920787

Mansano, S. Bagga and W. Serdijn, 2013. A high efficiency orthogonally switching passive charge pump rectifier for energy harvesters. IEEE Trans. Circuits Syst., 60: 1959-1966. DOI: 10.1109/TCSI.2012.2230499

Motiur Rahaman, D.M., M.S. Islam, J. Sampe and S.H.M. Ali, 2015. An architecture of ULP energy harvesting power conditioning circuit using piezoelectric transducer for wireless sensor network: A review. Asian J. Sci. Res., 8: 1-13. DOI: 10.3923/ajsr.2015.1.13

Nintanavongsa, P., U. Muncuk, D.R. Lewis and K.R. Chowdhury, 2012. Design optimization and implementation for rf energy harvesting circuits. IEEE J. Emerging Selected Topics Circuits Syst., 2: 24-33. DOI: 10.1109/JETCAS.2012.2187106

Nishimoto, H., Y. Kawahara and T. Asami, 2010. Prototype implementation of ambient RF energy harvesting wireless sensor networks. Proceedings of the IEEE Sensors, Nov. 1-4, IEEE Xplore Press, Kona, Hi., pp: 1282-1287. DOI: 10.1109/ICSENS.2010.5690588

Ouda, M.H., M. Arsalan, L. Marnat, A. Shamim and K.N. Salama, 2013. 5.2-GHz RF power harvester in 0.18-/spl mu/m CMOS for implantable intraocular pressure monitoring. IEEE Trans. Microwave Theory Techniques, 61: 2177-2184. DOI: 10.1109/TMTT.2013.2255621

Papotto, G., F. Carrara and G. Palmisano, 2011. A 90-nm CMOS threshold-compensated RF energy harvester. IEEE J. Solid-State Circuits, 46: 1985-1997. DOI: 10.1109/JSSC.2011.2157010

Park, G., T. Rosing, M. Todd, C. Farrar and W. Hodgkiss, 2008. Energy harvesting for structural health monitoring sensor networks. ASCE J. Infrastructure Syst., 14: 64-79. DOI: 10.1061/(ASCE)1076-0342

Parks, A.N., A.P. Sample, Z. Yi and J.R. Smith, 2013. A wireless sensing platform utilizing ambient RF energy. Proceedings of the IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications, Jan. 20-20, IEEE Xplore Press, Santa Clara, pp: 160-162. DOI: 10.1109/PAWR.2013.6490222

Ping-Hsuan, H. and C. Tao, 2013. An RF energy harvester with 35.7% PCE at PIN of -15 dBm. Proceedings of the Symposium on VLSI Circuits, Jun. 12-14, IEEE Xplore Press, Kyoto, pp: C224-C225.

Pradhan, S., Seong-Ro, L.S.K. Noh and D.Y. Choi, 2014. Comparative study of rectenna for electromagnetic energy harvesting. Int. J. Control Automation, 7: 101-113. DOI: 10.14257/ijca.2014.7.3.11

Roscoe, N.M. and M.D. Judd, 2013. Optimization of voltage doublers for energy harvesting applications. IEEE Sensors J., 13: 4904-4911. DOI: 10.1109/JSEN.2013.2278468

Sarker, M.R., S.H.M. Ali, M. Othman and M.S. Islam, 2011. Design a low voltage energy harvesting SoC system for ultra-low-power biomedical application. Aus. J. Basic Applied Sci., 5: 341-345.

Shiho, K., 2011. RF energy harvesting techniques for wirelessly powered devices. Proceedings of the IEEE MTT-S International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals, Aug. 24-25, IEEE Xplore Press, Daejeon, pp: 1-2. DOI: 10.1109/IMWS2.2011.6027184

Shokrani, M.R., M. Khoddam, M.N.B. Hamidon, N.A. Kamsani and F.Z. Rokhani *et al*., 2014. An RF energy harvester system using UHF micropower CMOS rectifier based on a diode connected CMOS transistor. Sci. World J., pp: 1-11. DOI: 10.1155/2014/963709

Shrivastava, R.D., D. Deshpande, L. Changzhi and R. Gale, 2013. An energy harvesting system using 3-stage voltage multiplier and MPVD charge pump for wireless sensor networks. Proceedings of the IEEE Topical Conference on Wireless Sensors and Sensor Networks, Jan. 20-23, Austin, IEEE Xplore Press, pp: 40-42. DOI: 10.1109/WiSNet.2013.6488627

Sim, Z.W., 2010. Compact patch antenna design for outdoor RF energy harvesting in wireless sensors networks. Progress Electromagnetics Res., 105: 273-294. DOI: 10.2528/PIER10052509

Sivaramakrishnan, A. and K.J. Jegadishkumar, 2011. A highly efficient power management system for charging mobile phones using rf energy harvesting. Int. J. Inform. Technol. Convergence Services, 1: 21-30. DOI: 10.5121/ijitcs.2011.1503

Stoopman, M., S. Keyrouz, H.J. Visser, K. Philips and W.A. Serdijn, 2014. Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters. IEEE J. Solid-State Circuits, 49: 622-634. DOI: 10.1109/JSSC.2014.2302793

Stoopman, M., S. Keyrouz, H.J. Visser, K. Philips and W.A. Serdijn, 2013. A self-calibrating RF energy harvester generating 1V at -26 dBm. Proceedings of the Symposium on VLSI Circuits, Jun. 12-14, IEEE Xplore Press, Kyoto, pp: C226-C227.

Swapna Kumar, S. and K.R Kashwan, 2013. Research study of energy harvesting in wireless sensor networks. Int. J. Renewable Energy Res., 3: 745-753.

Taris, T., V. Vigneras and L. Fadel, 2012. A 900MHz RF energy harvesting module. Proceedings of the 10th International New Circuits and Systems Conference, Jun. 17-20, IEEE Xplore Press, Montreal, pp: 445-448. DOI: 10.1109/NEWCAS.2012.6329052

Theilmann, P.T., C.D. Presti, D.J. Kelly and P.M. Asbeck, 2012. A μW complementary bridge rectifier with near zero turn-on voltage in SOS CMOS for wireless power supplies. IEEE Trans. Circuits Syst. I: Regular Papers, 59: 2111-2124. DOI: 10.1109/TCSI.2012.2185293

Visser, H.J. and R.J.M. Vullers, 2013. RF energy harvesting and transport for wireless sensor network applications: Principles and requirements. Proc. IEEE, 101: 1410-1423. DOI: 10.1109/JPROC.2013.2250891

Wahab, S.A., M.S. Bhuyan, J. Sampe and S.H.M. Ali, 2014. Parametric analysis of boost converter for energy harvesting using piezoelectric for micro devices. Proceedings of the IEEE International Conference on Semiconductor Electronics, Aug. 27-29, IEEE Xplore Press, Kuala Lumpur, pp: 525-528. DOI: 10.1109/SMELEC.2014.6920914

Yakovlev, A., S. Kim and A. Poon, 2012. Implantable biomedical devices: Wireless powering and communication. IEEE Commun. Magazines, 50: 152-158. DOI: 10.1109/MCOM.2012.6178849