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CHARACTERISTIC ANALYSIS OF DUAL GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR BY MATHEMATICAL MODELING

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ABSTRACT

In this study, the characteristics of DGMOSFET were obtained using mathematical modeling. The variations of characteristics were analyzed with different conditions into consideration. Different parameters behavior is analyzed, such as Transcapacitance variation with the gate voltage, threshold voltage variation with respect to lateral straggle parameter and temperature, mobile charge density variation is also analyzed and also the drain characteristics of the DGMOSFET. The maximum drain current is obtained as 40 mA. The work is done using SPICE simulation software. The results obtained are in greater coherence with previous theoretical investigations.

Keywords: DGMOSFET, Drain Current, Transconductance

1. INTRODUCTION

Researchers have been working on the performance of the devices from past two decades. DGMOSFET is one such milestone in the evolution of devices. Silicon on insulator technology is extremely attractive in terms of performance and advanced scalability. As compared to bulk silicon, the architecture of DGMOSFETs is more flexible because more parameters, such as thicknesses of film and buried oxide, substrate doping and back gate bias, can be used for optimization and scaling. It is well known that the short-channel effects are remarkably reduced in SOI films. Since bulk MOSFETs are expected to reach their limit for gate lengths below 30 nm (Chaudhry and Kumar, 2004; Brown *et al*., 2002), alternative architectures have been proposed to overcome their limitations. The Double-Gate (DG) transistor is considered one of the most promising devices for extremely scaled CMOS technology generations (Widiez *et al*., 2005).

Indeed, due to a good electrostatic control of the channel by the two gates, it is expected to provide smaller short-channel effects, near ideal sub-threshold slopes and higher drive currents when compared to single-gate transistors. Advantage of Double gate SOI MOSFET over conventional, Single Gate MOSFET can be described in terms of performance and potential for ultimate Scaling. The Peculiarity of DG-MOSFET is that the top and bottom gates are biased simultaneously to established equal surface potential VG1 = VG2, for identical gate oxides, Or VG1 = VG2 (tox1/tox2) to compensate for the difference in front and back oxide thickness (Widiez *et al*., 2005).

1.1. Theory

In a conventional, bulk-silicon microcircuit, the active elements are located in a thin surface layer and are isolated from the silicon body with a depletion layer of a p-n junction. The leakage current of this p-n junction exponentially increases with temperature and is responsible for several serious reliability problems. Excessive leakage currents and high power dissipation limit the operation of microcircuits at high temperatures. Parasitic n-p-n and p-n-p transistors formed in neighboring

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insulating tubs can cause latch-up failures and significantly degrade the circuit performance.

Silicon-on-insulator technology employs a thin layer of silicon isolated from a silicon substrate by a relatively thick layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances and thus, eliminates the possibility of latch-up failures. **Figure 1** shows the typical structure of DGMOSFET. The mathematical modeling (Jazaeri *et al*., 2013; Smith, 2008) of the device is explained as follows.

The Gaussian profile in the channel region is modelled as:

$$N_{SD}(x) = N_{SD}(P)e^{-x2} / 2\sigma_L^0$$

- NCD (P)-peak of gaussian profile = 1×10^{20} cm^{-3}
- The gate work fn is 4.6ev
- Degenerated doping value N_{de} -2.7×10^{19} cm^{-3}
- Parabolic potential distribution along the vertical direction:

$$\Psi(x, y) = a(x) + b(x)y + c(x)y^2$$

where, a(x),b(x),c(x) determined using boundary conditions continuity of electric flux at the S_i-S_{io2} interface $\Psi(x,0) = \alpha(x)$:

$$\Psi(x, t_{si}) = a(x) + b(x)t_{si} + c(x)t_{si}^2$$

$$\frac{\partial\Psi(x, y)}{\partial y} = b(x).1 + c(x).2y$$

$$\frac{\partial\Psi(x, y)}{\partial y}\Big|_{y=0} = b(x) + c(x)2y = b(x)$$

$$\frac{\partial\Psi(x, y)}{\partial y}\Big|_{y=t_{si}} = b(x) + c(x).2t_{si} = b(x) + 2c(x)t_{si}$$

Now:

$$\frac{\partial\Psi(x, y)}{\partial y}\Big|_{y-0} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{(\Psi f(x) - (V_{GS} - V_{fb})}{t_{\sigma x}}$$

$$\frac{\partial\Psi(x, y)}{\partial y}\Big|_{y-t} \frac{\varepsilon_{\sigma x}}{\varepsilon_{si}} \frac{((V_{GS} - V_{fb}) - \Psi b(x)}{t_{\sigma x}}$$

V_{GS} = Applied gate potential
V_{fb} = Flat band voltage
$\Psi f(x)$ = Front surface potentials
$\Psi b(x)$ = Back surface potentials

Solving Equation 1 and 8:

$$c(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}} \frac{((V_{GS} - V_{fb}) - \Psi f(x))}{t_{cx}}$$

For a weak inversion operation, the 2D poisson equation, at S_i-S_{io2} interface, considering lateral source drain profile:

$$\frac{\partial^2\Psi}{\partial x^2} + \frac{\partial^2\Psi}{\partial y^2} = \frac{qNa^-}{\varepsilon_{si}} - \frac{qN_{SD}^+(x)}{\varepsilon_{si}}$$

Na^- = Ionized acceptor concentration
$N_{SD}^+(x)$ = Ionized donor concentration

$$N_{SD^+(X)} = \frac{(N_{SD}(P)e^{\frac{-x^2}{2\sigma_L^2}} + N_{SD}(P)e^{\frac{-(Lg-x)^2}{2\sigma_L^2}}}{(1 + SD_e^{((EF-ED)/KT)})}$$

E_F = Fermi level
E_D = Donor level of $N_{SD}(X)$
E_F = $(E_g/2)$+KTIn($N_{SD}(X)/ni_{eff}$)

$$E_D = E_{geff} - EI \rightarrow \quad (1)$$

Ionization energy EI considering many body effects involving ionized donor –$\bar{e}$ interaction is:

$$E_{10} - (1^{-3}\sqrt{N_{SD}(X) / N_{de}} = El$$

For Arsenic:

$$E_{IO} - 0.054ev$$

Degenerated doping value:

$$N_{de} = 2.7\times10^{19} cm^{-3}$$

SD-spin degeneracy factor.
The effective intrinsic concentration:

$$n_{ieff} = \sqrt{ni^2 e^{\Delta Eg/KT}}$$

E_{geff} = E_g-$\Delta e_g \rightarrow$ effective bandgap
E_g = Band gap (silicone-1.17ev,1.11ev)
n_i = Carrier density of intrinsic semiconductor

Using the potential expression of (1) and the values of a(x),b(x),c(x), the poisson can be written as i.e.,:

$$\frac{\partial^2\Psi}{\partial x^2}+\frac{\partial^2\Psi}{\partial y^2}=\frac{qN_a^-}{\varepsilon_{si}}-\frac{qN_{SD}^+(X)}{\varepsilon_{si}}$$

$$\frac{\partial\Psi f(x)}{\partial x^2}-\frac{\Psi f(x)}{\lambda^2}=\frac{q(N_a^- - N_{SD}^+(X))}{\varepsilon_{si}}-\frac{(V_{GS}-V_{fb})}{\lambda^2}$$

where, natural length:

$$\lambda=\sqrt{(\varepsilon_{si}t_{si}t_{\sigma x})/(2\varepsilon_{\sigma x})}$$

$$t_{si}\rightarrow 2\text{to}3\ \text{nm}$$

$$t_{ox}\rightarrow 10\ \text{mm}-1.2\ \text{nm}$$

The solution of (9) can be carried out by calculating its complimentary fn and the particular integral.

Calculation of PI including the Gaussian term is mathematically very complex to implement in a compact model.

We have approximated the PI by considering the absolute value of Gaussian profile at each point of the channel.

The above equation can be written as:

$$\Psi f=C_{1e}^{-x/\lambda}+C_{2e}^{x/\lambda}+PI$$

Where:

$$PI=(V_{GS}-V_{fb})-\lambda^2 q\frac{(N_a^- - N_{SD}^+(x))}{\varepsilon_{si}}\rightarrow \quad (2)$$

C1,C2-calculated using boundary condition at effective S/D ends:

$$\Psi_f(S_{eff})=V_{bi}$$

$$\Psi_f(D_{eff})=V_{bi}+V_{DS}$$

The effective S/D ends are calculated when S/D doping concentration reaches the critical value of N_{de}:

$$S_{eff}\sqrt{\ln(N_{de}/N_{SD}(P))\times(-2\sigma_L^2)}\rightarrow \quad (3)$$

$$L_{eff}=L_g-2\times S_{eff}\rightarrow \quad (4)$$

$$D_{eff}=L_g-S_{eff}=S_{eff}+L_{eff}\rightarrow \quad (5)$$

$$C_1=\left(\frac{V_{bi}-C_2e^{S_{eff}/\lambda}-PI}{e^{-S_{eff}/\lambda}}\right)\rightarrow \quad (6)$$

$$C_2=\left(\frac{(V_{bi}-PI)\left(1-\left(e^{(-D_{eff}/\lambda)}\right)\Big/\left(e^{(-S_{eff}/\lambda)}\right)\right)+V_{DS}}{e^{D_{eff}/\lambda}-\left(e^{S_{eff}/\lambda}/e^{-S_{eff}/\lambda}\right)e^{\frac{-D_{eff}}{\lambda}}}\right)\rightarrow \quad (7)$$

Build in potential (V_{bi}) can be approximately used as:

$$V_{bi}:V_t\ln\left(\frac{N_{de}N_a}{n_{ieff}^2}\right)\rightarrow \quad (8)$$

$$V_t=K^T/q-\text{Thermalvoltage}$$

The min potential point:

$$x_{min}=\frac{\lambda}{2}\ln\left((C_1/C_2)_{max}\right)$$

Is calculated by equating:

$$\partial\Psi_f/\partial x=0$$

The threshold voltage is defined as the gate voltage when the channel τ densitives at the min potential point reach the channel doping density:

$$\left(ni^2/Na\right)e^{\left(\Psi_f(xmin)/V_t\right)}N_a$$

This yields the expression for V_t:

$$V_{th}=V_{fb}+2\phi-C_{1max}e^{\frac{-x_{min}}{\lambda}}-C_{2max}e^{\frac{x_{min}}{\lambda}}+\frac{\lambda^2 q\left(N_a^- - N_{SD}^+(x_{min})\right)}{\varepsilon_{si}}$$

Where:

$$n_i(T)=5.29\times10^{19}(T/300)^{2.54}\exp^{(-6726/T)}$$

$$\phi=V_t\ln(N_a/n_i)$$

$$n_i=8.3e^9cm^{-3}$$

$$T=298.15K$$

1.2. Dual Gate MOSFET

The concept of a Double-gate MOSFET is that it efficientlycontrols the channel from gates on both sides of the channelinstead of one gate in planar bulk MOSFETs. Controllingthe channel by multiple gates has its supremacy of better control over the channelinversion, so the short channel effect is reduced. Morespecifically, reducing the current leakage and eliminatingthe drain-induced barrier lowering effect areexamples of superiority in double-gate MOSFETs. (Antoniadis *et al*., 2006; Keyes, 1986; Mohapatra *et al*., 2012).

The new methodologies give rise to two paths; one is the introduction of new materials into the classical single gate MOSFETs where we can develop uniaxial/biaxial strain (Widiez *et al*., 2005; Smith, 2008; Vaddi *et al*., 2012) and which improves the carrier mobility and drive current by introducing new materials in the channel region. Second is the development of non-classical Multigate MOSFETs which is very good concept for further scaling of the device dimensions (Antoniadis *et al*., 2006; Keyes, 1986; Dunga *et al*., 2006). Kumar *et al*. (2007) had shown the effect of strain/Ge mole fraction on the threshold voltage for a single gate MOSFET. DG-MOSFETs have substituted traditional bulk MOSFETs, which suffer from severe second-order effects, such as short channel effects that result in performance loss (Young, 1989).

2. RESULTS

In this section, the results obtained by the mathematical modeling and simulation of the device structure shown in **Fig. 1** are presented.

Figure 2 represents the typical dual gate MOSFET and its operation.

Figure 3 represents the drain current variation with respect to the gate voltage and this graph represent the convention FET device characteristics, which is very encouraging. The maximum drain current value obtained in this case is 40 mA with a gate source voltage variation from 0 to 10V.

Figure 4 represents the mobile charge density variation with respect to lateral direction.

Figure 5 represents the threshold voltage variation with respect to the lateral straggle, a key parameter for a DGMOSFET structure characterization.

Figure 6 and 7 represents the Transcapacitance variation with the gate to source voltage for different doping concentration values and **Fig. 8** represents the effect of temperature on the threshold voltage of the device.

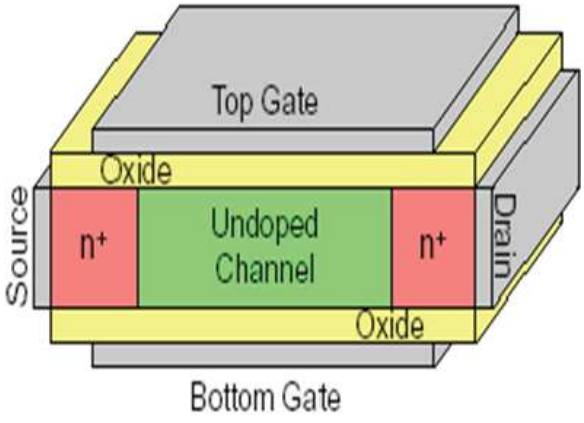

Fig. 1. Typical structure of DGMOSFET

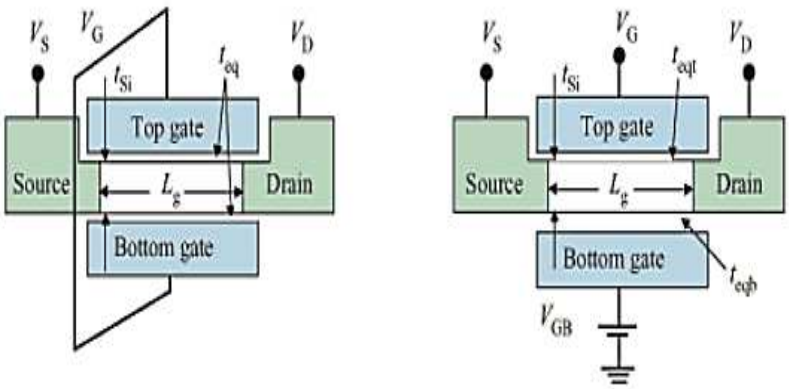

Fig. 2. Dual gate MOSFET operation

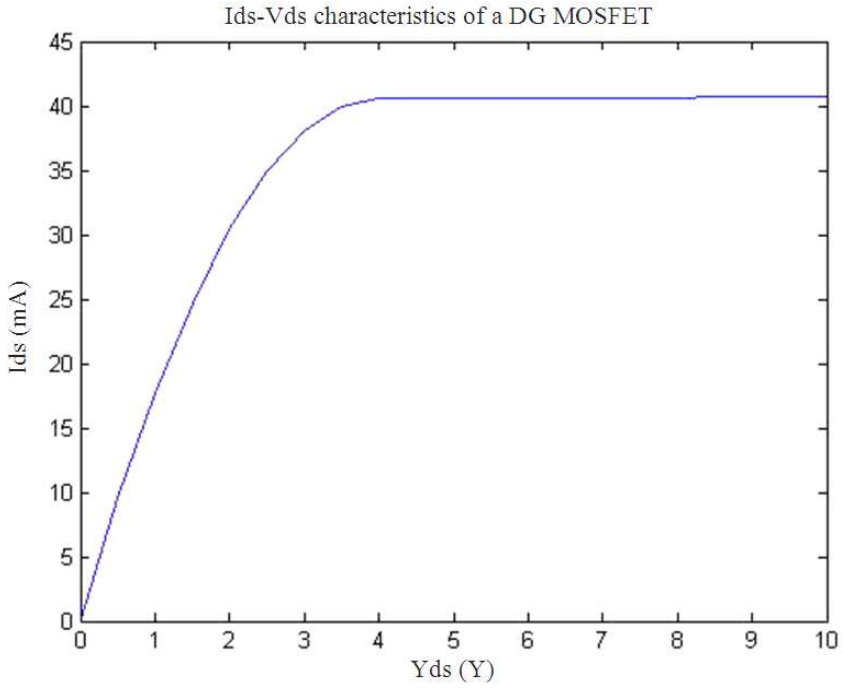

Fig. 3. Id VsVds Characteristics

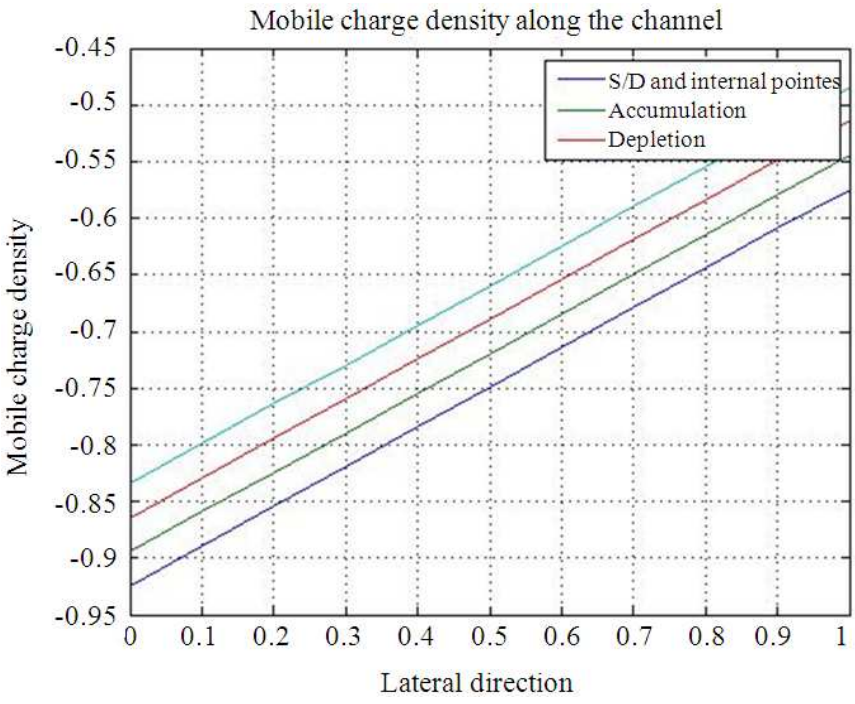

Fig. 4. Variation of mobile charge density

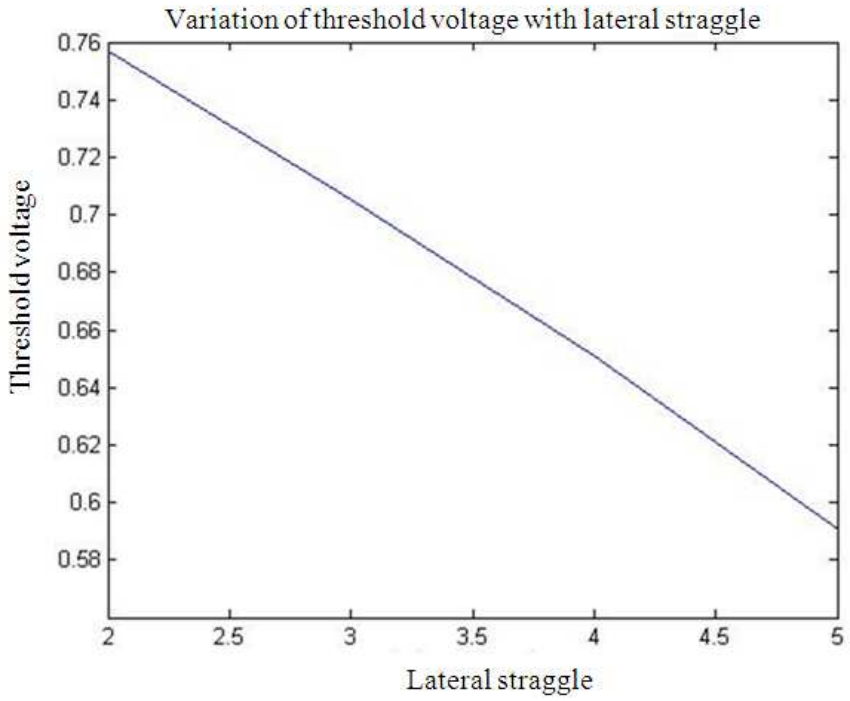

Fig. 5. Threshold voltage variation with lateral straggle

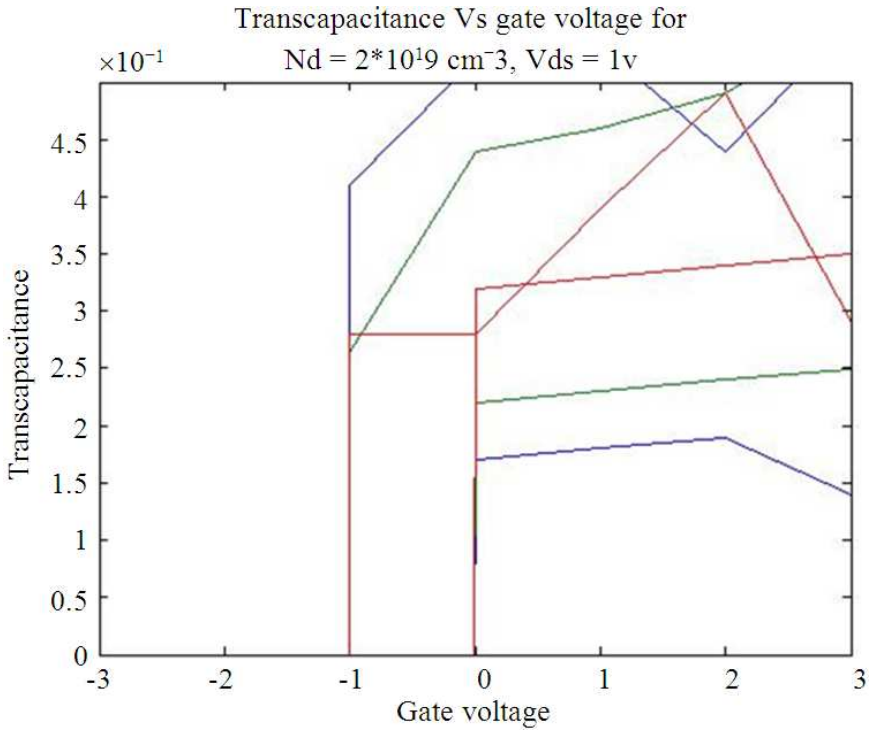

Fig. 6. Transcapacitance variation with gate voltage at nd1

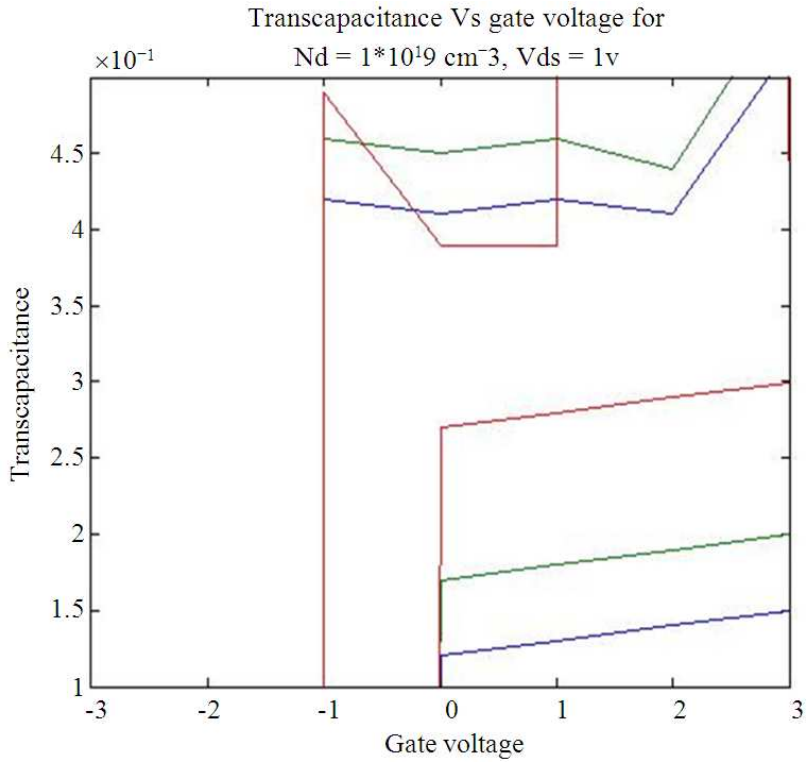

Fig. 7. Transcapacitance variation with gate voltage at Nd2

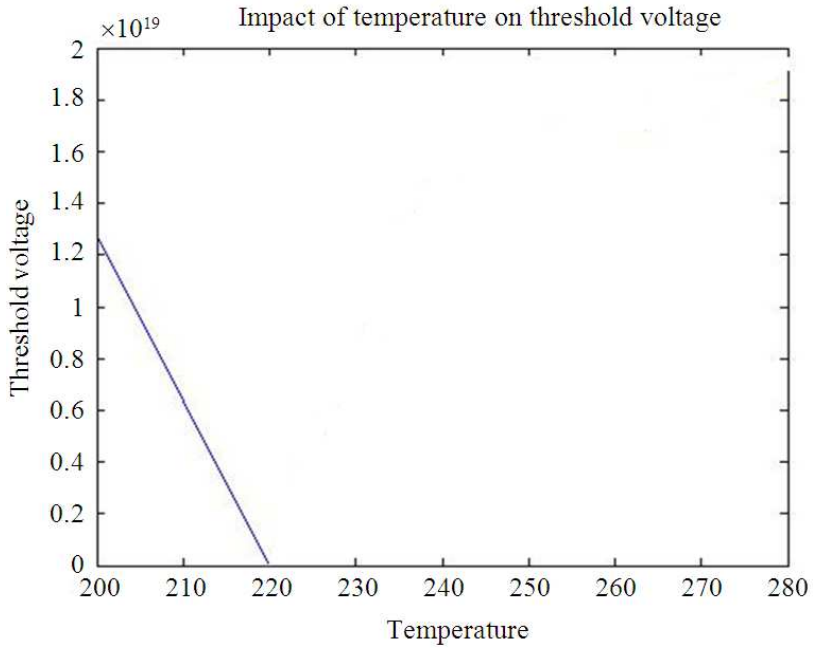

Fig. 8. Threshold voltage variation with temperature

3. CONCLUSION

The operation of DGMOSFET brings significant advantages: Scalability, high current drive, low short channel effects, excellent transconductance. The results represents the variation of the parameters like threshold voltage, Transcapacitance under different biasing and other constraints, this would necessarily establish their effect on the performance of the device, particularly in the device characteristics. This study can be extended for different illumination conditions of DGMOSFET, which may in turn increase the performance of the device.The futurescope of this study also exist in the comparative study of various multigate devices.

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