

A Novel Interconnect Structure for Elmore Delay Model with Resistance-Capacitance-Conductance Scheme

¹Uma Ramadass, ²Krishnappriya, ³Jebashini Ponnian and ¹P. Dhavachelvan

¹Department of Computer Science, School of Engineering, Pondicherry University, Pondicherry, India

²Department of Electronics, School of Engineering, Pondicherry University, Pondicherry, India

³Department of Electrical and Electronics, Infrastructure University Kuala Lumpur Kajang, Malaysia

Received 2013-04-12, Revised 2013-07-16; Accepted 2013-07-19

ABSTRACT

In this brief, we present a simple close-form delay estimate, based on first and second order moments that handle arbitrary voltages and conductance effects for a lumped and distributed line. This proposed model introduces a simple tractable delay formula by incorporating conductance (G) into Resistance, Capacitance (RC) network by preserving the characteristics of the Elmore delay model. The RCG model attains quick steady state condition and the accuracy of the interconnect delay estimates can be improved by deploying the conductance effect. The simulation results shows the proposed interconnect scheme performance is better than the existing in terms of delay, power and the figure of merit. The performance analysis depicts that the proposed scheme has improved its figure of merit with minimum and maximum of 21.12% and 49.13%. The analysis is validated through extensive simulations on a 250 nm CMOS technology.

Keywords: Elmore Delay, RCG Interconnect, RLC Network, Figure of Merit, Damping Ratio

1. INTRODUCTION

Increasing demand in circuit compaction, speed and high level of integration entail an accurate interconnect models to verify the performance and functionality of VLSI circuits. Generally the interconnects are modeled through three electrical parameters namely the Resistance (R), Capacitance (C) and Inductance (L).

The conventional approach used to determine the signal delay for both analog and digital circuits by using Elmore delay (also called classical delay model). The main limitation to this model is inaccurate and the analysis is limited to estimate the delay of the circuit for the first order moments. These classical problems has been surrogated through compound interest problem to the existing Elmore delay to improve the efficiency of the RC interconnect scheme. The modified Elmore delay model through compound interest has been reported by (Avci and

Yamacli, 2010). Albeit this scheme improves accuracy but the estimation is restricted for RC network alone. Mal and Dhar (2010) has reported a dominant pole delay model by fixing the resistance and capacitance value for estimating the delay of arbitrary RC network. This model provides delay accuracy to the first order RC network.

The Bond Graph (BG) energy model with a Simulink Energy Based Block Diagram (SEBD) algorithm has been developed by (Chang *et al.*, 2011). This approach resolves the model approximations in RLC Very Large Scale Integration (VLSI) interconnect network systems. The higher order approximation produces inaccuracy which is the general limitation in this approach. Beta Distribution function based closed form Delay Metric model for the RC trees has been proposed by (Kar *et al.*, 2010a). The mathematical model has low computation complexity, but lacks in accuracy.

Corresponding Author: Uma Ramadass, Department of Computer Science, School of Engineering, Pondicherry University, Pondicherry, India

Moment matching approach has been developed by (Alioto, 2011) which includes the analysis of input admittance of RC interconnects. This model determines first and higher order moments of RC networks. Their approach incorporates fully analytical and lacks certain constraints for CAD issues. Rajib Kar *et al.* (2010b) proposed a unified approach for estimating the interconnect delays by fitting the moments for impulse response by taking probability density function to estimate the delay and slew accurately. The moments are matched using Fisher-Snedecor distribution (F Distribution) approximation, which has two parameter (positive poles D1 and D2) continuous distributions that can be matched for generalized RC network to characterize the complete model. This approximation is used for both step and ramp type signals but not suitable for second order systems for calculating the moments.

An analytical timing model for inductance-dominant interconnects using traveling wave propagation and perturbation technique has been proposed by (WenDing and GaofengWang, 2009). The proposed model is theoretically stable but produces non-monotonic characteristics. The model proposed by (Maheshwari *et al.*, 2011) evaluates the performance of an interconnect by deploying the property of conductance to improve the characteristics properties of delay. A delay model for RLC trees based on algebraic equations and an algorithm has been proposed based on the lie formula (Roy and Dounavis, 2011). Though the model can be applied to step and ramp input type of signals, it is inefficient for second order delay modeling and limited to only first two circuit moments.

Moment based Delay Modeling for On-Chip RC Global VLSI Interconnect were also introduced by developing Two pole RC model based on first, second and third moment effect into the delay estimate for interconnect lines (Halder *et al.*, 2012). This model takes higher order circuit moments for accuracy in delay, but it is not applicable for second order systems. A simple explicit delay and rise time approach has been proposed by (Datta *et al.*, 2010) for an n-cell RC uniformly distributed ladder network with capacitive load. This model is limited only for RC network.

The literature survey reported in this study focus only on the interconnect delay model involving resistance, capacitance and inductance effects. But as the technology scales down the significant of conductance plays a vital role for improving the device performance as well as in delay aspect. This study presents a new Modified Elmore model (MEDL) which incorporates

the effect of conductance to improve the delay for lumped and distributed interconnect networks.

2. MATERIALS AND METHODS

The most commonly used method to evaluate the transient response for RC network is an Elmore delay model. The model estimates the delay of the networks as the sum of each capacitance times the resistance through which it must be charged or discharged. This interconnect delay models a wire as a segment of resistance and capacitance which is connect in series as shown in **Fig. 1**. The method employed to obtain the transfer function in this model is based on simple circuit analysis. First the transfer function of the ladder is obtained with one R and one C element in the circuit. Then using a recursive node approach, the voltage transfer function of next higher node is derived in-terms of its previous and successive node. The process is continued till the final output node is reached and the transfer function relating output node voltage and input node voltage is obtained. The Elmore delay equation explains the delay from input to output, which is of a step function type. If the step response of the RC circuit is $h(t)$, 50% point delay of the monotonic step response is the time τ_n that satisfies the Equation (1).

The delay for a lumped RC interconnects is modeled as the time constant (τ) of an RC interconnect. So the delay for a lumped RC interconnect is:

$$\tau = RC \quad (1)$$

The delay for the distributed RC interconnect is modeled as the total sum of the delay in each node Equation (2-4):

$$\text{Delay at node 1 : } \tau_1 = R_1 C_1 \quad (2)$$

$$\text{at node 2 (N2) : } \tau_2 = (R_1 + R_2) C_2 \quad (3)$$

$$\text{Delay at node 3 (N3) : } \tau_3 = (R_1 + R_2 + R_3) C_3 \quad (4)$$

In general the delay for the distributed RC network is calculated as Equation (5):

$$\tau_n = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + \dots + (R_1 + R_2 + \dots + R_n) C_n \quad (5)$$

If $R_1 = R_2 = \dots = R_n = R$ and $C_1 = C_2 = \dots = C_n = C$, then the delay is modeled as Equation (6):

$$\tau_n = RC + 2RC + \dots + nRC \quad (6)$$

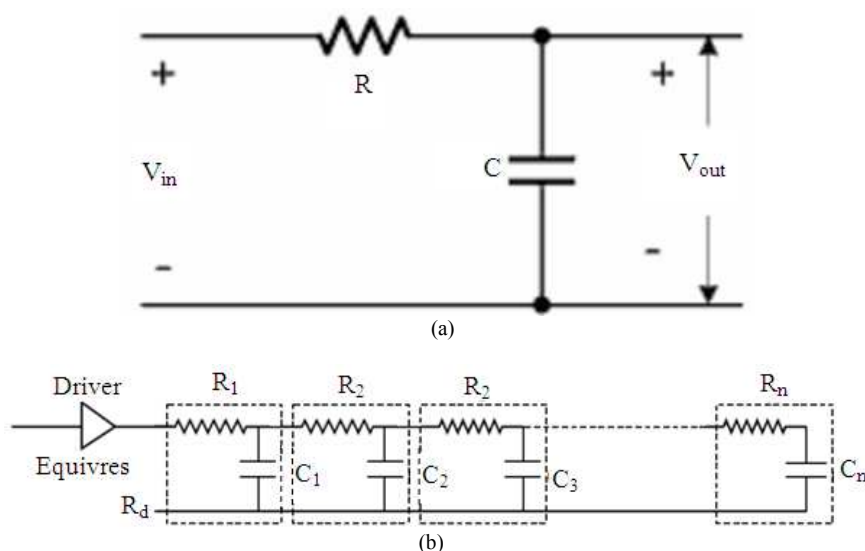


Fig. 1. Elmore interconnect scheme. (a). Lumped model (b). Distributed network

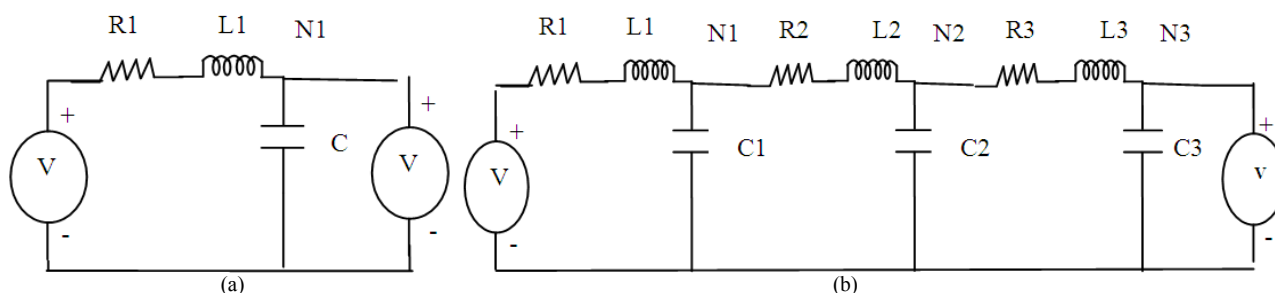


Fig. 2. RLC interconnect scheme. (a). Lumped model (b). Distributed network

The demerits of using this Elmore delay model are: Practical difficulties in obtaining the poles and residues for long interconnect. This method is applicable for obtaining the first order moments. The method produces inaccurate approximation for higher order moments. The model lacks to capture the effect of inductance in the interconnect model and accuracy gets decline in case of increased clock frequencies.

Practically the interconnects includes the effects of inductance. So an RLC interconnect models are employed to improve the accuracies of two-pole model. The delay model gains higher accuracy than RC due to the second order moment capturing effect of the inductance. An effective analysis for structural modelling using Bond Graph (BG) energy model with a Simulink Energybased Block Diagram (SEBD) algorithm has been proposed for RLC tree network

systems (Chang *et al.*, 2011). The lumped and distributed RLC model is shown in **Fig. 2**.

The delay for a lumped RLC interconnects is modeled as the time constant of an RLC interconnect. So the delay for a lumped RLC interconnect is Equation (7):

$$\tau = 2L/R \tag{7}$$

The delay of the distributed RLC interconnect is modeled as the total sum of the delay in each node Equation (8):

$$\tau_n = \frac{2L}{R} + \frac{R^2 + RL + 2L}{R} + \frac{2R^2 + 2RL + 2L}{R} + \frac{nR^2 + nRL + 2L}{R} \tag{8}$$

The major problem associated with RLC models are: Applicable only to step type functions and does not characterize the overshoots and settling time of an under damped response. Calculation of real, complex and multiple poles requires higher order differential equations. Moreover the characteristics of RLC model does not focuses on closed-form solutions for the moments of an interconnect tree. Extraction of inductance in practical 3-D interconnect geometry are complex and time consuming process. As inductance depends on the entire current loop it is impractical for extracting the inductance from the chip layout. The primary focus of this study is to introduce a simple tractable delay formula for RCG network by preserving the characteristics of the Elmore delay model with improved accuracy in the interconnect delay scheme (model).

2.1. Proposed RGC Delay Model

The proposed work presents a simple closed form delay modeling for first and second order moments to handle arbitrary voltages and conductance effects for a lumped and distributed interconnect network . A plain tractable delay estimate has been formulated by incorporating conductance (G) effect into RC network thereby preserving the properties of Elmore delay model. This Modified Elmore Delay Model (MEDL) with RCG interconnect considers a uniform wire that is schematized as lumped or distributed RCG network whose total resistance $R_{total} = \rho L/W$ and capacitance $C_{total} = \beta LW$ which is proportional to its length L. The RCG network is modelled as:

- In the proposed interconnect scheme drivers (buffers) are included in the root nodes. Various loading capacitances are also included in the interconnect model
- The transfer functions for first and second order moments are calculated from source to sink using recursive approach
- Resistance along each segment i related to, $R_i \propto 1/w_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment
- Capacitance along each segment i related to, $C_i \propto w_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment
- Conductance along each segment i related to, $G_i \propto w_i/L_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment, $L_i \rightarrow$ length of the wire along i^{th} segment
- In the interconnect scheme R_p , C_p and G_p represents the resistance, capacitance and conductance of the proposed interconnect scheme

The delay estimates for lumped network is shown in **Fig. 3**. To estimate the delay for lumped model the transfer function of simple RCG ladder is calculated. The delay equation is derived by taking input voltage (V_1) and output voltage (V_O) is time dependent function which is of linear differential equation.

From output side equation we obtain the transfer function as Equation (9-11):

$$V_O(S) = \frac{(1/C_p S) \parallel G_p}{R_p + (1/C_p S) \parallel G_p} V_1(S) \tag{9}$$

$$\frac{V_O(s)}{V_1(S)} = \frac{1}{(1 + (R_p / G_p) + R_p C_p S)} \tag{10}$$

$$H(S) = \frac{1}{(R_p / G_p + 1)(R_p C_p S G_p / R_p + G_p) + 1} \tag{11}$$

Taking inverse Laplace for the transfer function results in Equation (12 and 13):

$$H(j\omega) = \frac{1}{\sqrt{R_p C_p \omega^2 + 1}} \tag{12}$$

$$H(j\omega) = \frac{1}{\sqrt{\frac{\omega^2}{\omega_1^2} + 1}} \tag{13}$$

$\tau = \frac{R_p C_p G_p}{(R_p + G_p)}$ is the change in the output voltage $V_o(t)$ is delayed by the time constant Equation (14):

$$\tau_{propRCG} = \frac{R_p C_p G_p}{(R_p + G_p)} \text{ for lumped model} \tag{14}$$

For distributed network the entire interconnect is divided into various segments. **Figure 4** shows the proposed distributed model. The delay for above distributed network is modelled as the total sum of the delay in each node Equation (15-17):

$$\text{Delay at node 1: } \tau_1 = \frac{R_{p1} C_{p1} G_{p1}}{(R_{p1} + G_{p1})} \tag{15}$$

Delay at node 2 : $\tau_2 = \frac{R_{p1} + R_{p2}C_{p2}G_{p2}}{(R_{p2} + G_{p2})}$ (16)

$\tau_n = \frac{1}{R_p + G_p} (R_p C_p G_p + 2R_p C_p G_p + \dots + nR_p C_p G_p)$ (18)

Delay at node 3 : $\tau_3 = \frac{R_{p1} + R_{p2} + R_{p3}C_{p3}G_{p3}}{R_{p3} + G_{p3}}$ (17)

The second order model for the proposed interconnect scheme is obtained by making G_1 is parallel to C_1 so for simplification it is represented as X. Similarly G_2 is parallel to C_2 for simplification it is represented as Y. The simplified second order moment is shown in Fig. 5.

In general the delay for the distributed RC network is calculated as Equation (18):

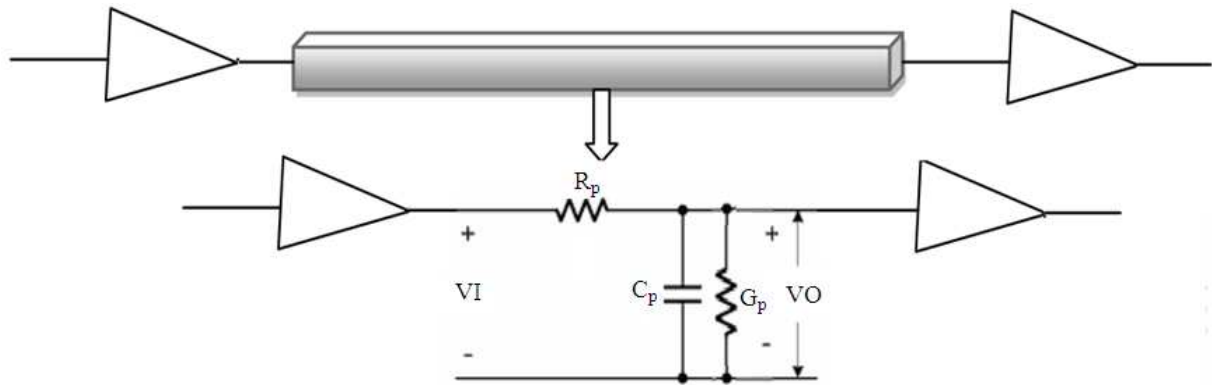


Fig. 3. Proposed RCG lumped model

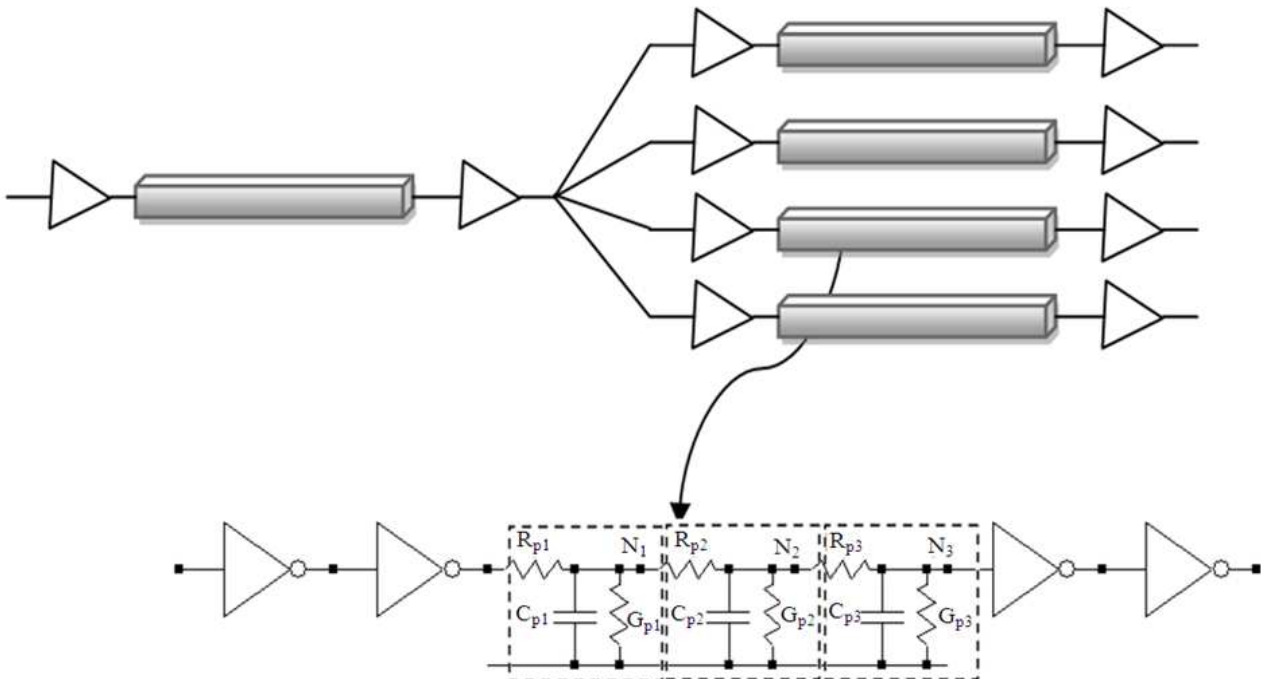


Fig. 4. Proposed RCG distributed model

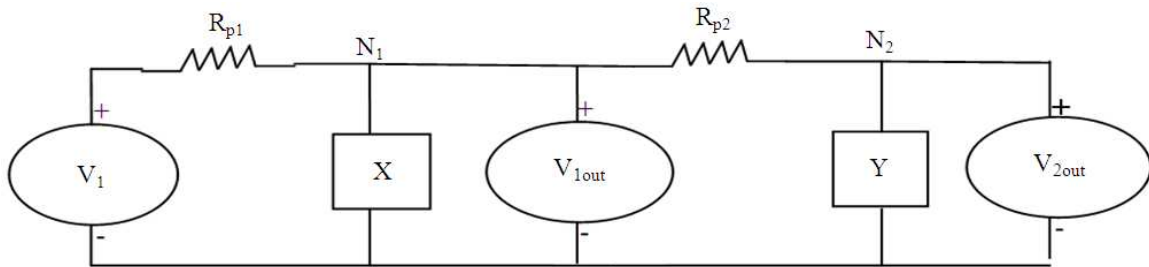


Fig. 5. Second order model for proposed RCG model

In second order model, G_1 is parallel to C_1 so for simplification X is modeled as Equation (19):

$$X = G_{p1} \parallel \frac{1}{SC_{p1}} \Rightarrow X = \frac{\frac{G_{p1}}{SC_{p1}}}{G_{p1} + \frac{1}{SC_{p1}}} \quad (19)$$

$$\Rightarrow X = \frac{G_{p1}}{SC_{p1}G_{p1} + 1}$$

G_2 is parallel to C_2 , so Y is modeled as Equation (20):

$$Y = G_{p2} \parallel \frac{1}{SC_{p2}} \Rightarrow Y = \frac{\frac{G_{p2}}{SC_{p2}}}{G_{p2} + \frac{1}{SC_{p2}}} \quad (20)$$

$$\Rightarrow Y = \frac{G_{p2}}{SC_{p2}G_{p2} + 1}$$

V_{1out} , the output voltage at node1 is calculated using the voltage divider rule with respect to the input voltage applied Equation (21):

$$V_{1out} = \frac{XV_1}{R_{p1} + X}$$

$$V_{1out} = \frac{\left(\frac{G_{p1}}{SG_{p1}C_{p1} + 1}\right)V_1}{R_{p1} + \frac{G_{p1}}{SG_{p1}C_{p1} + 1}} \quad (21)$$

$$V_{1out} = \frac{G_{p1}V_1}{SG_{p1}C_{p1}R_{p1} + R_{p1} + G_{p1}}$$

V_{2out} , the output voltage at node2 is calculated using the voltage divider rule with respect to input voltage applied Equation (22):

$$V_{2out} = \frac{YV_{2in}}{R_{p1} + Y}$$

$$V_{2out} = \frac{\left(\frac{G_{p2}}{SC_{p2}G_{p2} + 1}\right)\left(\frac{G_{p1}V_1}{SG_{p1}C_{p1}R_{p1} + R_{p1} + G_{p1}}\right)}{R_{p1} + \frac{G_{p2}}{SC_{p2}G_{p2} + 1}} \quad (22)$$

The closed loop transfer function of a second order system can be written as Equation (23):

$$\frac{V_{2out}}{V_1} = \frac{G_{p1}G_{p2}}{(SR_{p2}C_{p2}G_{p2} + R_{p2} + G_{p2})(SG_{p1}C_{p1}R_{p1} + R_{p1} + G_{p1})}$$

$$H(S) = \frac{G_{p2}G_{p1}}{S^2G_{p1}C_{p1}R_{p1}G_{p1}C_{p1}R_{p1} + SR_{p2}C_{p2}G_{p2}(R_{p1} + G_{p1}) + SG_{p1}C_{p1}R_{p1}(R_{p2} + G_{p2}) + (R_{p2} + G_{p2}) + R_{p1} + G_{p1}}$$

$$H(S) = \frac{1}{S^2 + \frac{C_{p1}R_{p1}C_{p2}R_{p2}}{S(R_{p2}C_{p2}G_{p2}(R_{p1} + G_{p1}) + R_{p1}C_{p1}G_{p1}(R_{p2} + G_{p2}))} + \frac{R_{p2}C_{p2}G_{p2}R_{p1}C_{p1}G_{p1}}{(R_{p1} + G_{p1})(R_{p2} + G_{p2})} + \frac{R_{p2}C_{p2}G_{p2}R_{p1}C_{p1}G_{p1}}{R_{p2}C_{p2}G_{p2}R_{p1}C_{p1}G_{p1}}}$$

By comparing the above equation with the characteristic equation, given in the form:

$$S^2 + 2\zeta\omega_n + \omega_n^2$$

We obtain the values of ω_n & ζ Equation (24 and 25):

$$\omega_n = \sqrt{\frac{(R_{p1} + G_{p1})(R_{p2} + G_{p2})}{R_{p2}C_{p2}G_{p2}R_{p1}C_{p1}G_{p1}}} \quad (24)$$

$$\zeta = \frac{1}{2} \frac{R_{p2}C_{p2}G_{p2}(R_{p1} + G_{p1}) + R_{p1}C_{p1}G_{p1}(R_{p2} + G_{p2})}{\sqrt{R_{p2}C_{p2}G_{p2}R_{p1}C_{p1}G_{p1}(R_{p1} + G_{p1})(R_{p2} + G_{p2})}} \quad (25)$$

Table 1. Damping ratio and Delay for RC ,RLC and Proposed RCG

RC	$\frac{1}{2} \frac{R_1 C_1 + R_2 C_2}{\sqrt{R_1 C_1 R_2 C_2}}$
Damping ratio RLC	$\frac{1}{2} \frac{RC}{\sqrt{LC}}$
Proposed RCG	$\frac{1}{2} \frac{R_{p2} C_{p2} G_{p2} (R_{p1} + G_{p1}) + R_{p1} C_{p1} G_{p1} (R_{p2} + G_{p2})}{\sqrt{R_{p2} C_{p2} G_{p2} R_{p1} C_{p1} G_{p1} (R_{p1} + G_{p1}) (R_{p1} + G_{p1})}}$
Delay RC	$\frac{2R_1 C_1 R_2 C_2}{R_1 C_1 + R_2 C_2}$
RLC	$\frac{2LC}{RC}$
Proposed RCG	$\frac{2R_{p2} C_{p2} G_{p2} R_{p1} C_{p1} G_{p1}}{R_{p2} C_{p2} G_{p2} (R_{p1} + G_{p1}) + R_{p1} C_{p1} G_{p1} (R_{p2} + G_{p2})}$

Where

ω_n is the natural frequency

ξ is the damping ratio, is a parameter characterizes the frequency response of a second order differential equation and it is a measure of how rapidly the oscillations decay from one bounce to the next. The delay can be calculated from the below Equation (26):

$$\tau = \frac{1}{\xi \omega_n} \tau = \frac{2R_{p2} C_{p2} G_{p2} R_{p1} C_{p1} G_{p1}}{R_{p2} C_{p2} G_{p2} (R_{p1} + G_{p1}) + R_{p1} C_{p1} G_{p1} (R_{p2} + G_{p2})} \quad (26)$$

The above derived equation is the delay equation of the second order MEDL model. The damping ratio and delay expression for the proposed RCG MEDL, RC and RLC interconnect scheme is shown in **Table 1**.

3. RESULTS

To test the performance of the proposed and existing interconnects TANNER ASIC-EDA tool has been used. All the interconnects are based on TSMC 0.250 μm technology with supply voltage ranging from 1.2 to 5 V in steps of 0.2 V. The model is simulated by taking typical values of resistance $R_p = 15 \text{ k}$, capacitance $C_p = 2 \text{ pf}$ and conductance $G_p = 0.05 \text{ mS}$ for lumped and distributed interconnects. For the proposed RCG interconnects the longer wires has been partition into shorter sections to maintain the signal integrity and to reduce the total propagation delay. Buffers are inserted to main the signal level throughout the longer interconnects. The interconnects

are simulated with a 100MHz clock frequency. Input signal is unit step signal and the delay estimates refer to 50% threshold voltage. The minimum cross section for RC and RLC has been taken as 0.33 and 0.18 μm . The transient response for the proposed lumped and distributed RCG interconnect are shown in **Fig. 6 and 7**. The time response is analyzed for the step response of 200 ns with input voltage of 5 v and output response obtained is an exponential curve.

The experimental results shows the output transient response for step input is faster for the proposed RCG interconnect scheme when compared to its counterpart. For various values of R, G and C the delays are obtained for lumped and distributed model through simulation and theoretically which are reported in **Table 2 and 3**.

The proposed interconnect scheme is simulated for various voltages by keeping R, C and G constant and its delay, average power and figure of merit are reported in **Table 4**. For this observation R_p value is taken as 15 k Ω and C_p value is 2 pf and conductance is 0.05 mS. The relative utilization of the interconnect scheme to characterize the device performance is define as figure of merit. This parameter has been calculated as product of delay and average power. The minimum voltage and maximum voltage applied for this interconnect are 1.8 to 5 V. The rise time is calculated for a waveform to rise from 10 to 90% of its steady-state value. The fall time is calculated for a waveform to fall from 90 to 10% of its steady-state value. The percentage improvement for the proposed and existing counterpart is elucidated in **Table 5**.

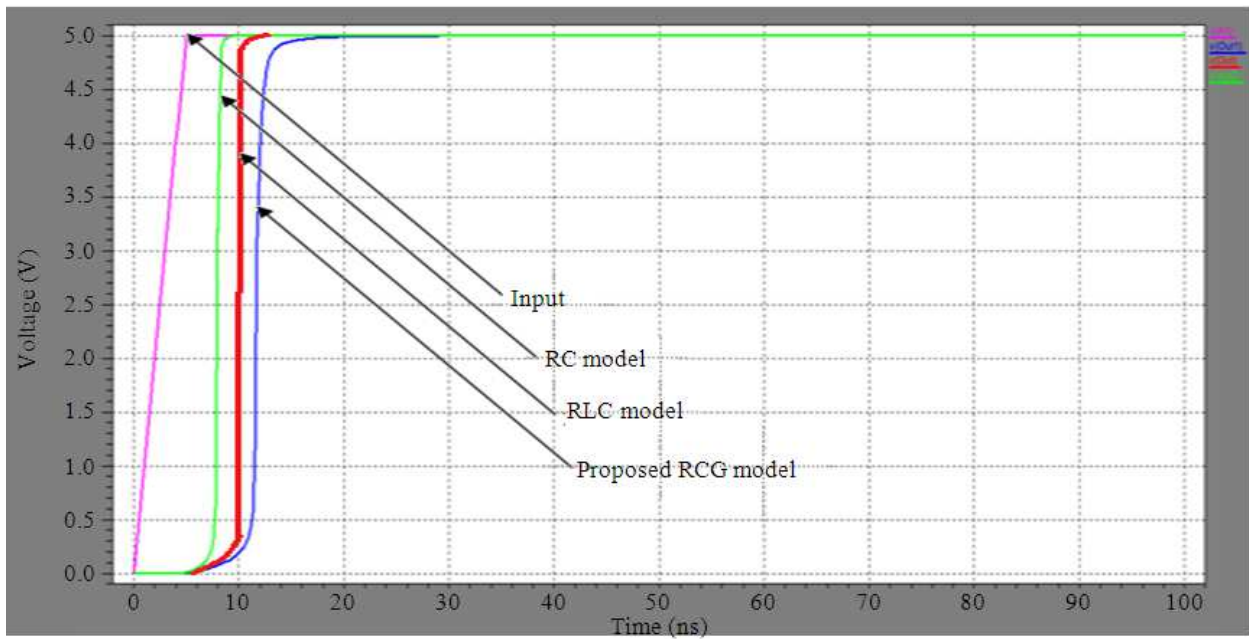


Fig. 6. Simulation results for proposed RCG lumped model

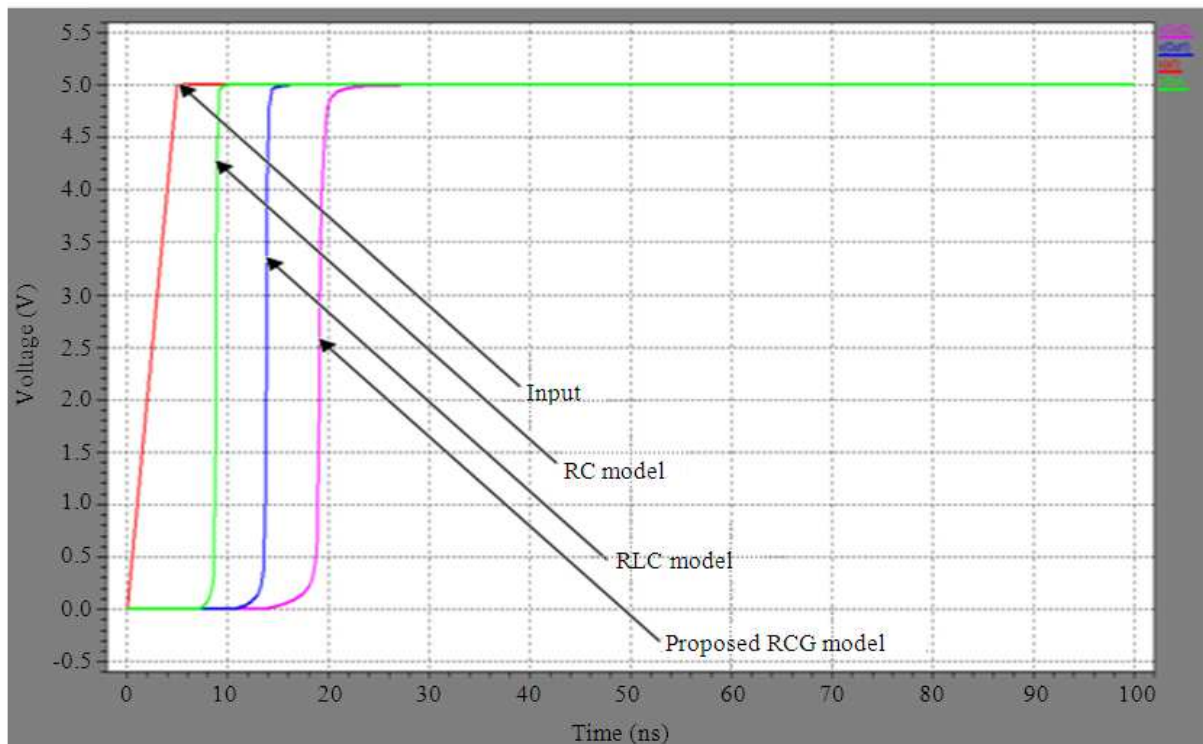


Fig. 7. Simulation results for proposed RCG distributed model

Table 2. Delay obtained for Various R, C and G for lumped model

R (kΩ)	C (pf)	G (mS)	Theoretical delay (nS)	Simulated delay (nS)
25	2	0.05	22.22	22.488
20			20.00	18.844
15			17.14	13.642
10			13.33	10.459
5			08.00	07.336
1			01.90	01.119
15	1	0.05	08.57	06.781
	3		25.70	24.564
	5		42.85	41.767
	7		60.00	58.582
	10		85.71	86.430
15	2	0.09	12.69	13.413
		0.08	13.33	14.486
		0.07	14.48	15.123
		0.06	15.48	13.548

Table 3. Delay obtained for Various R, C and G for distributed model

R ₁ = R ₂ (kΩ)	C ₁ = C ₂ (pf)	G ₁ = G ₂ (mS)	Theoretical delay (nS)	Simulated delay (nS)
25	2	0.05	22.22	22.370
20			20.00	19.798
15			17.14	17.251
10			13.33	15.082
5			08.00	09.597
1			01.90	02.963
15	1	0.05	08.57	07.914
	2		25.70	24.510
	3		42.85	40.964
	4		60.00	58.795
	5		85.71	82.004
15	2	0.08	12.69	12.811
		0.07	13.33	14.990
		0.06	14.48	14.224
		0.04	15.48	16.885
		0.03	17.83	18.377

4. DISCUSSION

This study presents a new proposed interconnect scheme RCG model. Simulation results proves the superiority of the proposed interconnect scheme in terms of delay, power and figure of merits with its counter part. **Table 5** depicts the progressive improvements of delay, power and figure of merit for various voltages for constant values of R, C and G. The interconnects are simulated with a 100MHz clock frequency with minimum cross section of 0.33 and 0.18μm. The minimum voltage and maximum voltage applied for this interconnect are 1.8V to 5V with step input of time period 100ns. From **Table 5** it is noticed that the percentage of delay is much improved for RC

model and RLC interconnect model. For the lumped RC model with minimum voltage of 1.8V, the delay factor has improved to 19.3 and 39.5% improvement when the supply voltages reaches 4.6V keeping all the values of R, C and G as constant. Similarly for distributed network there is 20.9 to 39.5% improvement attained for the input voltage of 1.8 to 5 V. For RLC lumped model the minimum improvement is 24.37% to a maximum of 39.9%. The delay percentage variation is depicted in **Fig. 8**. From this graph it is observed that for the proposed lumped model the delay is linear for the voltages ranging from 1.8 to 5 v. In the proposed distributed model for 1.8V the delay is maximum and remains constant as voltages are increased.

Table 4. Simulated results for power and figure of merit obtained for various voltages

Interconnect scheme	Type of interconnect	Voltages (v)	Delay (ns)	Rising time (ns)	Fall time (ns)	Power (μ w)	Figure of merit $\times 10^{-6}$
lumped model	RC [1]	1.8	20.655	1.0908	8.3775	0.497	10.26
		2.4	21.017	2.7473	7.1463	0.483	10.15
		3.5	19.931	4.4083	7.2432	0.470	09.36
		4.6	21.755	2.1003	7.3825	0.469	10.20
		5.0	20.138	3.4520	7.4481	0.451	09.08
	RLC [3]	1.8	22.677	1.1055	8.3773	0.553	12.54
		2.4	23.027	2.7925	7.1461	0.543	12.50
		3.5	21.931	4.4351	7.2430	0.534	11.71
		4.6	23.447	1.5336	7.3874	0.526	12.33
		5.0	22.137	3.4586	7.4487	0.517	11.44
	RCG [prop]	1.8	16.660	1.0858	1.0635	0.486	08.09
		2.4	14.959	3.5979	5.4576	0.474	07.09
		3.5	13.392	5.255	4.9913	0.465	06.22
		4.6	14.202	4.7948	0.9436	0.453	06.43
		5.0	13.641	4.6805	2.1703	0.448	06.11
distributed model	RC [1]	1.8	43.730	6.0549	6.7719	0.586	25.62
		2.4	42.985	1.1955	6.1418	0.573	24.63
		3.5	43.357	1.6499	6.3977	0.561	24.32
		4.6	43.342	2.6997	6.4449	0.554	24.01
		5.0	42.564	3.3273	2.8894	0.546	23.23
	RLC [3]	1.8	45.714	6.0333	6.7706	0.599	27.38
		2.4	44.960	1.1944	6.1376	0.586	26.34
		3.5	45.347	1.4887	6.3948	0.575	26.07
		4.6	46.321	3.0818	6.4495	0.562	26.03
		5.0	44.527	3.3744	2.1114	0.551	24.53
	RCG [prop]	1.8	34.571	5.4672	2.1563	0.463	16.00
		2.4	30.421	2.8189	2.1428	0.474	14.41
		3.5	28.128	3.3510	2.1684	0.476	13.38
		4.6	27.821	2.9454	1.0584	0.476	13.24
		5.0	27.251	4.7939	0.8993	0.483	13.16

Table 5. Percentage improvement in delay, power and figure merit for the proposed RCG

Interconnect scheme	Voltages(v)	Overall improvement with respect to Proposed RCG in terms of different voltages		
		% improvement in delay	% improvement in power	% improvement in figure of merit
Lumped model w.r.t RC	1.8	19.34	2.21	21.15
	2.4	28.82	1.86	30.14
	3.5	32.80	1.06	33.54
	4.6	34.71	3.41	36.96
	5.0	32.26	0.66	32.70
Lumped model w.r.t RLC	1.8	26.53	12.11	35.48
	2.4	35.03	12.70	43.28
	3.5	38.93	12.92	46.88
	4.6	39.52	13.87	47.85
	5.0	38.37	13.34	46.59
Distributed model w.r.t RC	1.8	20.94	20.98	37.54
	2.4	29.22	17.27	41.49
	3.5	35.12	15.15	44.98
	4.6	35.81	14.07	44.85
	5.0	35.97	11.53	43.34
Distributed model w.r.t RLC	1.8	24.37	22.70	41.56
	2.4	32.33	19.11	45.29
	3.5	37.97	17.21	48.67
	4.6	39.93	15.30	49.13
	5.0	38.79	12.34	46.35

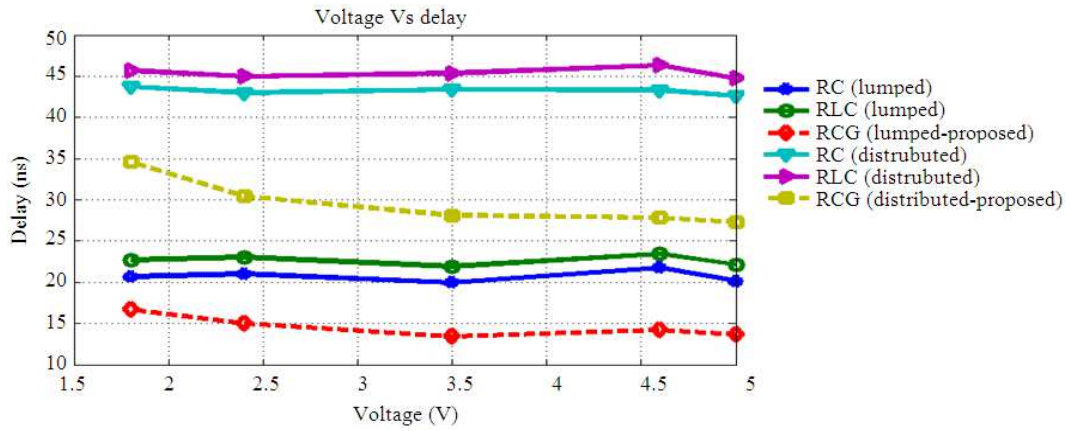


Fig. 8. Delay comparison chart

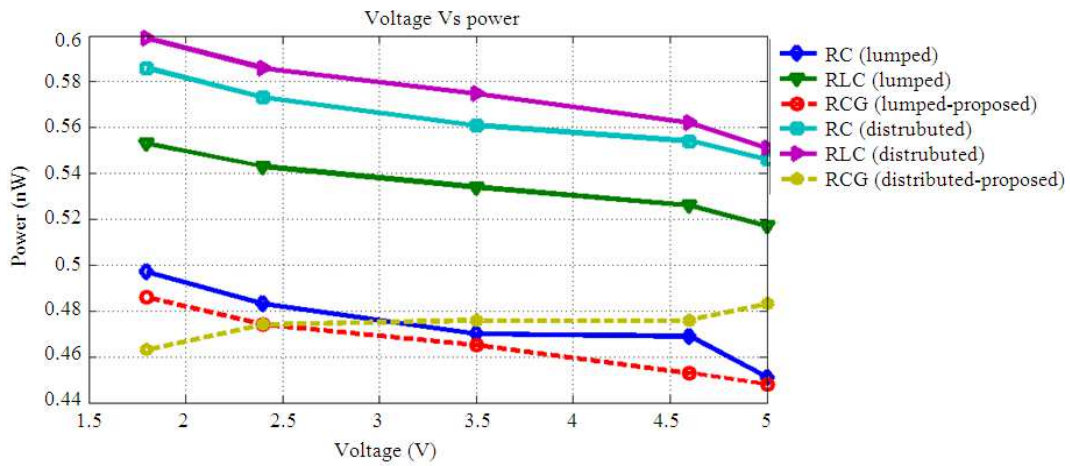


Fig. 9. Power comparison chart

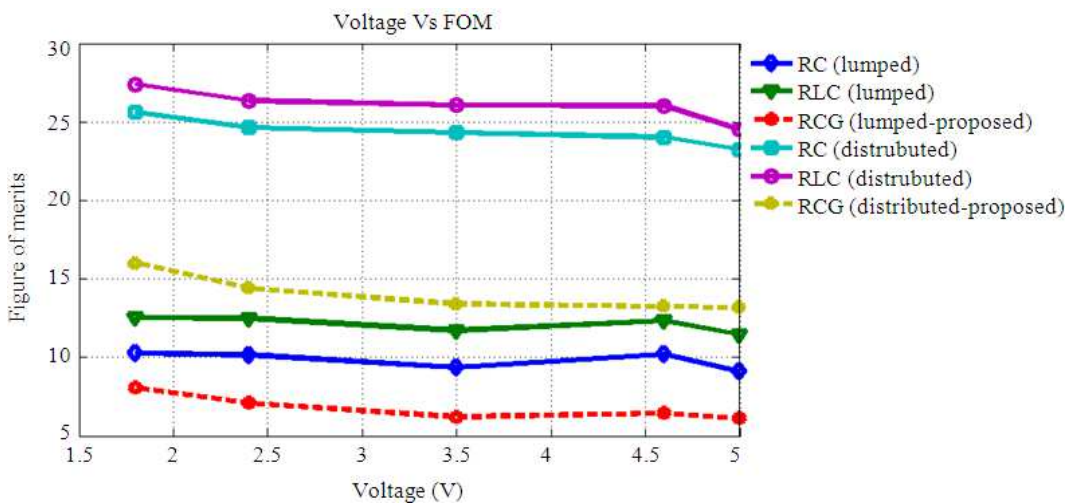


Fig. 10. Figure of merit comparison chart

The power comparison is shown in **Fig. 9**. From this graph it is noticed that for the proposed lumped model the power consumption is reduced as voltages are increased, while for distributed network the power consumption has negative characteristics when compared to proposed lumped model. The minimum power consumption is observed to be 1.06% and maximum of 22.7%. The figure of merit graph is shown in **Fig. 10**. This graph shows there is a linearity characteristic for both proposed lump and distributed model. The minimum and maximum figure of merit is 21.12% and 49.13%. So from this analysis it is well-tactic that the proposed model performs better than its existing counterparts for the lumped and distributed networks.

5. CONCLUSION

A new closed form delay equation using RCG interconnect scheme has been proposed for lumped and distributed model by taking second order moments into account. The simulation results show the proposed interconnect scheme performance is better than the existing interconnect scheme in terms of delay, power and the figure of merit. The performance analysis depicts that the proposed scheme has improved its figure of merit with minimum and maximum of 21.12 and 49.13%. The power consumption has been observed to be linear for the proposed model with minimum of 1.06% and maximum of 22.7%. While comparing delay the minimum has been observed to be 19.3% and maximum improvement of 39.9%. Comparisons on performance analysis shows that the RCG interconnect scheme to be more efficient than the existing counterparts. The model proposed will be suitable for applying in larger circuit may show significant improvement in delay and power.

6. REFERENCES

- Alioto, M., 2011. Modeling strategies of the input admittance of RC interconnects for VLSI CAD tools. *Microelectron. J.*, 42: 63-73. DOI: 10.1016/j.mejo.2010.09.003
- Avci, M. and S. Yamacli, 2010. An improved Elmore delay model for VLSI interconnects. *Math. Comp. Model.*, 51: 908-914. DOI: 10.1016/j.mcm.2009.08.024
- Chang R.F., W.S. Kao, C.W. Chang, K.H. Tseng and S.Y. Huang, 2011. A novel structural modeling and analysis of VLSI interconnect with an RLC tree network system using a BG/SEBD approach. *Sci. China Inform. Sci.*, 54: 1968-1985. DOI: 10.1007/s11432-011-4287-7
- Datta, M., S. Sahoo and R. Kar, 2010. An explicit model for delay and rise time for distributed RC on-chip VLSI interconnect. *Proceedings of the International Conference on Signal and Image Processing*, Dec. 15-17, IEEE Xplore Press, Chennai, pp: 368-371. DOI: 10.1109/ICSIP.2010.5697500
- Halder, A., V. Maheshwari, A. Goyal and R. Kar, 2012. Moment based delay modelling for on-chip RC global VLSI interconnect for unit ramp input. *Proceedings of the 9th International Joint Conference on Computer Science and Software Engineering*, May 30-Jun. 1, IEEE Xplore Press, Bangkok, pp: 164-167. DOI: 10.1109/JCSSE.2012.6261945
- Kar, R., V. Maheshwari, A. Mandal, A.K. Mal and A. Bhattacharjee, 2010a. Closed form modelling for delay and slew metrics for on-chip VLSI RC interconnect for ramp inputs using F-distribution. *Proceedings of the IEEE Symposium on Industrial Electronics and Applications* Oct. 3-5, IEEE Xplore Press, Penang, pp: 526-531. DOI: 10.1109/ISIEA.2010.5679407
- Kar, R., V. Maheshwari, S. Pathak, M.S.K. Reddy and A.K. Mal *et al.*, 2010b. An explicit approach for delay evaluation for on-chip RC interconnects using beta distribution function by moment matching technique. *Proceedings of the IEEE International Conference on Recent Trends in Information, Telecommunication and Computing*, Mar. 12-13, IEEE Xplore Press, Kochi, Kerala, pp: 5-8. DOI: 10.1109/ITC.2010.11 10.1109/ICCD.2002.1106806
- Maheshwari, V., A. Sharma, D. Mandal, R. Kar and A.K. Bhattacharjee, 2011. Transient and delay analysis for on-chip high speed VLSI RLCG interconnection network in 0.18 μm technology. *J. Electron Devices.*, 11: 554-559.
- Mal, A.K. and A.S. Dhar, 2010. Modified elmore delay model for VLSI interconnect. *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems*, Aug. 1-4, IEEE Xplore Press, Seattle, pp: 793-796. DOI: 10.1109/MWSCAS.2010.5548693
- Roy, S. and A. Dounavis, 2011. Efficient delay and crosstalk modeling of RLC interconnects using delay algebraic equations. *IEEE Trans. Large Scale Integrat. Syst.*, 19: 342-346. DOI: 10.1109/TVLSI.2009.2032288
- WenDing and GaofengWang, 2009. Analytical timing model for inductance-dominant interconnect based on traveling wave propagation. *Microelectron. J.*, 40: 905-911. DOI: 10.1016/j.mejo.2008.11.061