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# NOVEL REVERSIBLE VARIABLE PRECISION MULTIPLIER USING REVERSIBLE LOGIC GATES

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## ABSTRACT

Multipliers play a vital role in digital systems especially in digital processors. There are many algorithms and designs were proposed in the earlier works, but still there is a need and a greater interest in designing a less complex, low power consuming, fastest multipliers. Reversible logic design became the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In this study a reversible logic gate based design of variable precision multiplier is proposed which have the greater efficiency in power consumption and speed since the partial products received are accumulated as soon as they are computed which results reduction in the need of memory.

**Keywords:** Reversible Logic Gates, Variable Precision Multiplier, Quantum Computing, VLSI, Multipliers

## 1. INTRODUCTION

Designing of digital systems are highly influenced by the speed of computation and power consumption by the logic circuit used in it. Most of the time the improvement in the design is based on these parameters only. Power consumption is more critical area where the concentration is more to reduce it. As demonstrated by Landauer (1961), irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss. Also prove that Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Hence, another scientist Bennett (1973) showed that the circuit built using reversible logic gates are capable of avoid energy dissipation of order KTln2 joules. This study presents design of reversible variable precision multiplier with the help of reversible multiplier, reversible adder and reversible shift register. The paper is organized as follows section II presents the literature survey on reversible logic gates, section III and IV presents the concepts of variable precision representation and classical multiplication, section V presents the variable precision multiplication, section VI presents the proposed reversible variable precision multiplier and finally section VII presents the conclusion.

## 2. REVERSIBLE LOGIC GATES

Reversible logic has received significant attention in recent years. It has applications in various research areas:

- A function f: An→Am over the variable X = {x1, x2,…,xn} is reversible if it satisfies the following conditions
- Number of input and number of output must be equal
- Each input pzatterns maps to a unique output patterns

A reversible circuit is one which constructed by cascading of reversible gates. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback (Feynman, 1985; Mahammad and Veezhinathan, 2010; Perkowski and Kerntopf, 2001; Saravanan and Manic, 2013a; 2013b; Smith, 2003; Sreerama *et al*., 2012; Toffoli, 1980). It is important to consider the number of Garbage output, number of reversible gates, total delay and number of constant inputs while designing reversible logic circuit which decides the performance of the circuit the different types reversible logic gates available is listed in **Fig. 1**.

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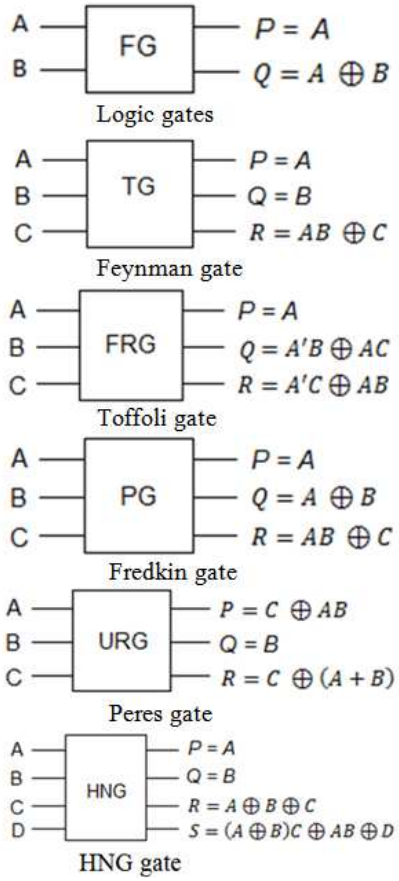


**Fig. 1.** List of existing reversible

## 3. VARIABLE PRECISION FLOATING POINT REPRESENTATION

The format of Variable Precision Floating Point representation is shown in **Fig. 2**. It consists of 16 bit exponent Field (E), one Sign bit (S), two bits to represent Type field (T), five bit to specify Length (L) and L+1 significant Field (F). The exponent is represented as two's complement integer, whether thenumber is normalized, infinite, zero or not a number is represented in the type field.

## 4. CLASSIC MULTIPLICATION METHOD

In the classical method of multiplication additions were carried out after obtaining all partial products. This method of multiplication needs adder, multiplier and accumulator of larger bit size. Not only the accumulator needed to be large the memory needed to store all the partial product till last one is computed then it proceed for addition and accumulation. If the size of the operant increases then the complexity multiplies to larger extent.

## 5. VPBFP MULTIPLICATION

Multiplication carried out by this algorithm is based on, multiplying two larger numbers A and B using smaller multiplications i.e., the multiplier and multiplicand are splitted into two parts LSP and MSP results into m-bits and also it reduces the memory that is used to store the partial products as soon as they are computed. this method needs only (n×2 m) memory bits. The number of memory locations needed and size of multiplier is based on m value. the flow of VPBFP is show in **Fig. 3**.

## 6. PROPOSED REVERSIBLE VPBFP MULTIPLIER

Designing of reversible logic circuit is challenging task, since not enough number of gates was available for design. Reversible processor design needs its building blocks should be reversible in this view the designing of reversible VPBFP multiplier became essential one.

In the proposed method the given multiplier and multiplicand is split into two parts with the size of 3bit each, the splitted part is forwarded to Reversible Multiplier one by one where the partial products are calculated and send immediately to Reversible Adder where it is accumulated and then send to memory and made it ready for next accumulation through Reversible Shift register but in case of classic method the partial products are stored in a memory continuously till last one is calculated then it send for accumulation here the proposed method differs and lead to less memory utilization and faster calculation, also the use of reversible circuit ensures the less power consumption the block arrangement of proposed method is shown in **Fig. 4**.

So this proposed algorithm will be faster than the classic multiplier and also it will have all the advantage of karatsuba algorithm. Since there are many optimal circuits are already proposed for Reversible multiplier, Reversible adder and Reversible shift register, the best among available is used in our design. While selecting the RA, RM, RSR its garbage's, number of LUT's and its power consumptions are considered.

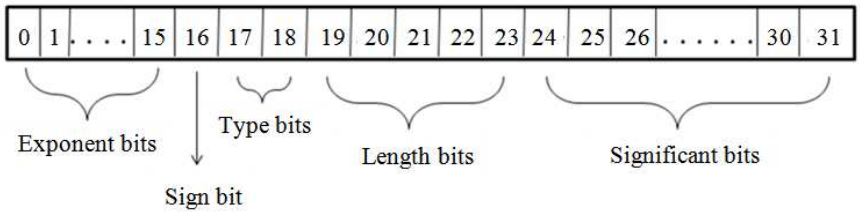


**Fig. 2.** Variable precision floating point representation

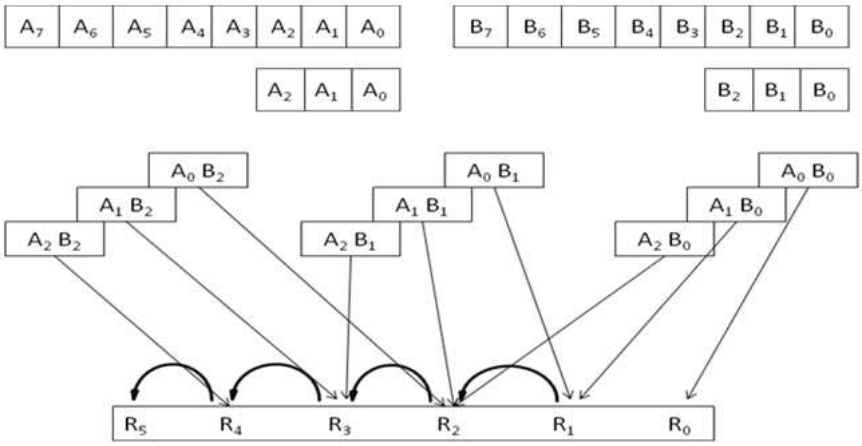


**Fig. 3.** Flow of VPBFP multiplier

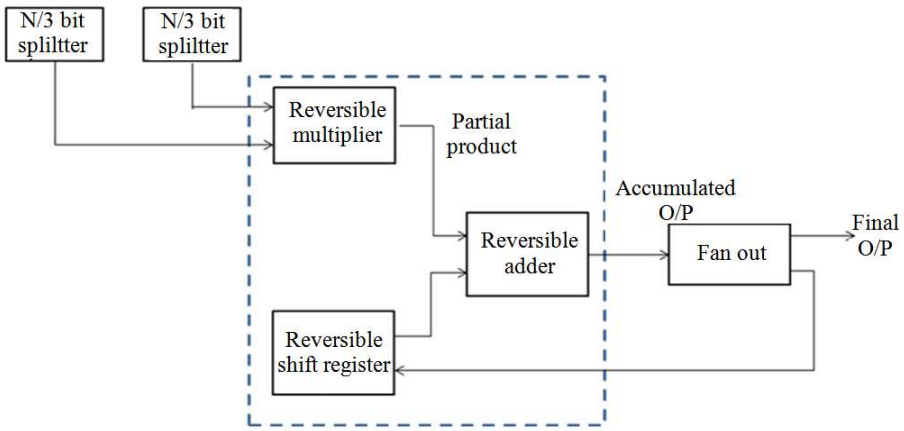


**Fig. 4.** Block diagram of reversible VPBFP multiplier

## 7. CONCLUCION

This study proposed a better performing multiplier design for high speed, less memory utilization and low power consumption, the proposed method has added advantages of karatsuba and VPBFP algorithms. The design was tested using VHDL. Since the availability of reversible logic gates are very few, if there is a development in getting more reversible logic gates then it is possible to achieve even better performance than this, proposed design is suitable to be used in application like high speed processing unit, DSP processors.

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