

# Gate Replacement Technique for Reducing Leakage Current in Wallace Tree Multiplier

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## ABSTRACT

Leakage power has become more significant in the power dissipation of today's CMOS circuits. This affects the portable battery operated devices directly. The multipliers are the main key for designing an energy efficient processor, where the multiplier design decides the digital signal processors efficiency. In this study gate replacement technique is used to reduce the leakage power in 4×4 Wallace tree multiplier architecture which has been designed by using one bit full adders. This technique replaces the gate which is at worst leakage state by a library gate. In this technique the actual output logic state is maintained in active mode. The main objective of our study is to calculate leakage power in 4×4 Wallace tree multiplier by applied gate replacement technique and it is compared with 4×4 Wallace tree full adder multiplier. The proposed method reduces 43% of leakage power in 4×4 Wallace tree multiplier.

**Keywords:** Leakage Current, Wallace Multiplier, Gate Oxide, Full Adder, Subthreshold Leakage

## 1. INTRODUCTION

The multipliers play a major role in arithmetic operations in digital signal processing applications. The present development in processor design aim at low power multiplier architecture usage in their processor circuit. So the need for the low power multipliers has been increased. In past, device density and operating frequency were low enough, also that it was not a constraining factor in chips. When the scale of integration improves, more transistors, faster and than their predecessors are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation, stated by Drakasan *et al.* (1992). There are three main sources for leakage current:

- Source/drain junction leakage current
- Gate dielectric tunneling leakage
- Subthreshold leakage through the channel of an off transistor

The junction leakage occurs from the source or drain to the substrate through the reverse-biased diodes when

transistor is OFF. The magnitude of the diode's diffusion and leakage current density, which in turn, determined by the process technology.

The gate direct tunneling leakage flows from the gate through the "leaky" oxide insulation to the substrate. Its magnitude increases exponentially with the gate oxide thickness and supply voltage VDD.

The subthreshold current is the drain-source current of an OFF transistor. This is due to the diffusion current of the minority carriers in the channel for MOS device operating in the weak inversion region.

In this study, we present a gate replacement technique that reduces the overall leakage power in 4×4 Wallace tree multiplier. The focus of this study is on leakage current reduction in standby mode of operation by replacing gates at worst leakage state.

## 2. MATERIALS AND METHODS

Here we briefly survey the different techniques used to reduce leakage power in 4×4 Wallace tree multiplier. Many techniques thus have been proposed recently to reduce the leakage power consumption.

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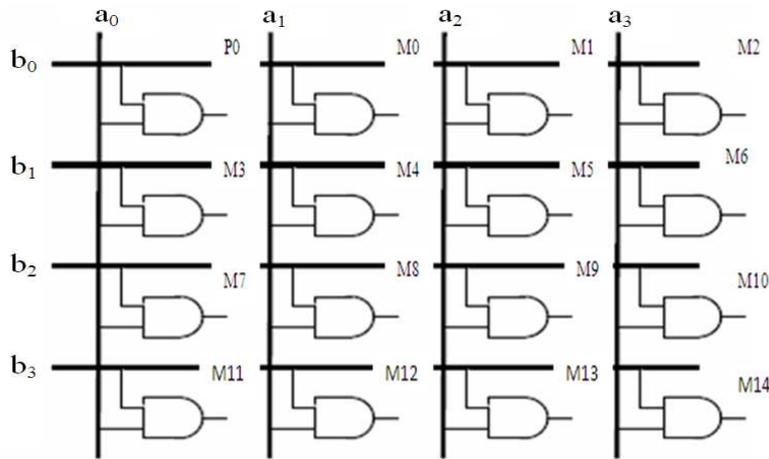


Fig. 1. AND gate generating input to multiplier block

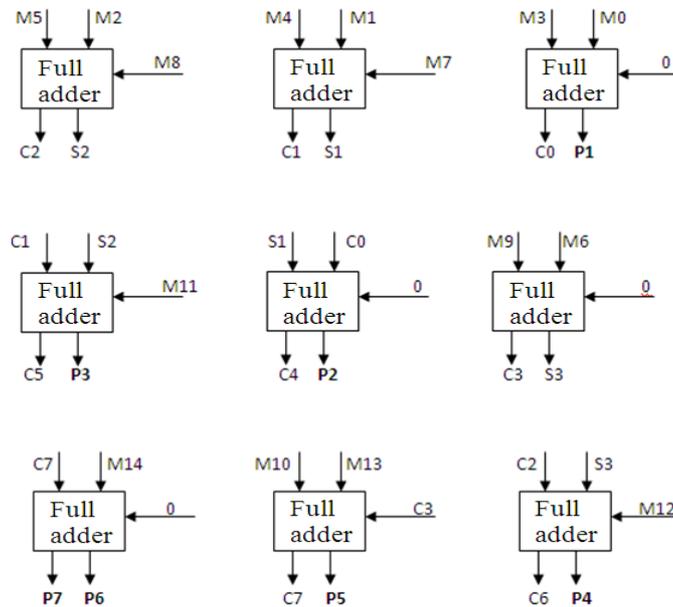


Fig. 2. Multiplier diagram being designed using full adder

Khandelwal *et al.* (2005) reported that dual threshold voltage process uses devices with higher threshold voltage along noncritical paths to reduce leakage current while maintaining the performance.

Khandelwal and Srivastava (2004) stated that Multiple Threshold CMOS (MTCMOS) technique places a high  $V_{th}$  device in series with low  $V_{th}$  circuitry, creating a sleep transistor Assaderaghi *et al.* (1997) reported that, in the dynamic threshold MOS(DTMOS), the gate and body are tied together and the threshold

voltage is altered dynamically to suit the operating state of the circuit. Another technique proposed by Kuroda *et al.* (1996) is to dynamically adjust the threshold voltage in the Variable Threshold CMOS (VTCMOS). Thus in all the above techniques there is a requirement of process technology support.

Another technique for leakage power control is power-gating approach proposed by Agarwal *et al.* (2006). This technique turns off the devices by cutting of their supply voltages. Moreover, bulky PMOS and/or

NMOS devices (sleep transistors) are introduced in between either supply or ground and circuit. Introduction of sleep transistors creates virtual power and ground rails in the circuit. The sleep transistor is turned on while circuit is in active state and turned off when circuit is in idle mode. This is done with the help of sleep signals.

Yuan and Qu (2006) reported that the Input Vector Control (IVC) technique is applied to reduce leakage current at circuit level with little or no performance overhead. Recently Lee *et al.* (2003) observed that gate oxide leakage is also dependent on the input vectors to a CMOS gate. Besides, the maximum and minimum leakage vectors are same for both subthreshold leakage and gate leakage.

The 4x4 Wallace tree multiplier with full adder method replaces the full adders in the place of half adders. So there is no need for separate final summing system as shown in **Fig. 1 and 2**. Hence the total leakage power is reduced, which is stated by Radhakrishnan (2001).

In this study we present a gate replacement technique to reduce the leakage power in 4x4 Wallace tree multiplier. Experiment results obtained from the proposed method described later in this study is compared with 4x4 Wallace tree multiplier with full adder.

**2.1. Proposed Work**

A 4x4 Wallace tree multiplier circuit is designed using 2-input NAND gate. The circuit is sufficiently large consisting of 12 full adders. When designed with only NAND gate it has 266 2-input NAND gate, totaling of 1064 transistor. In our method, We use cadence spectra to measure the overall leakage current in a CMOS gate that includes both subthreshold leakage and gate leakage. The below shown **Table 1 and 2** lists the overall leakage current in 2-input NAND and 3-input NAND gate.

**2.2. Gate Replacement Technique**

The essence of gate replacement technique is to replace a logic gate which is at its Worst Leakage State (WLS) by another library gate.

**2.3. Algorithm for Searching and Replacing Gates at WLS**

- Step 1: for each gate  $G, \sum \{G1, G2, \dots\}$
- Step 2: if ( $G_i$  is at WLS and not marked)
- Step 3 : include  $G_i$  in the selection  $S$ ;
- Step 4: while (there is new addition to  $S$ )
- Step 5: for each newly selected gate  $G$  in  $S$
- Step 6: if (there exists library gate  $\hat{G}$  meets the condition to reduce leakage)

- Step 7: temporarily replace  $G$  by  $\hat{G}$ ;
- Step 8: if (output of  $G$  is changed due to replacement)
- Step 9: include  $G$ 's unmarked fanout gate  $G_j$  in  $S$ ;
- Step 10: compute total leakage change of gates in  $S$ ;
- Step 11: if (there is leakage reduction)
- Step 12: mark all gates  $G_j$  in the section  $S$ ;
- Step 13: make replacement in lines 7, 9 or 10 permanent;
- Step 14: else mark gate  $G_i$  only;
- Step 15: empty the section  $S$
- Step 16: else mark  $G_i$  if it has not been marked yet;

This algorithm is used to search the worst leakage gate in 4x4 Wallace tree multiplier. It find the 2-input NAND gates at worst leakage state and replaces them by 3-input library NAND gate. This technique introduce a sleep signal at the worst leakage gate. The complement of the sleep signal will be given as the third input to the 2-input NAND gate during standby mode of operation. So the output is not affected during active mode of operation because sleep signal signal value is logic one. By comparing **Table 1 and 2** it shows that by given complement of sleep signal as the third input for the 2-input NAND gate the leakage current is drastically reduced during the standby mode of operation. By reducing leakage current in worst leakage state gates the overall leakage current in 4x4 Wallace tree multiplier is reduced.

**Table 1.** Leakage values for 2-input NAND gate

Input	Leakage (nA)
00	37.84
01	100.30
10	95.17
11	454.50

**Table 2.** Leakage values for 3-input NAND gate

Input	Leakage (nA)
000	22.84
001	37.84
010	37.84
011	100.30
100	37.01
101	95.17
110	94.87
111	852.40

**Table 3.** Comparison table

Leakage current for 100 nm process with VDD =1 Volt	
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Base case	Gate replacement technique
8.9000 E-07	4.2800 E-07

### 3. RESULTS

The gate replacement technique was implemented and tested on 4×4 Wallace tree multiplier using full adders. Hence we use cadence spectra using 100 nm to measure the overall leakage current in 4×4 Wallace tree multiplier. This technique provides 43% of reduction in leakage current when compared to the base case.

### 4. DISCUSSION

Here gate replacement technique is compared with the 4×4 Wallace tree multiplier with full adder.

From **Table 3** it is shown that 43% of leakage current is reduced by using gate replacement technique.

### 5. CONCLUSION

The leakage current of 4×4 Wallace tree multiplier was reduced by replacing half adders by full adders. But the leakage current was high during the standby mode of operation. In order to reduce this leakage current, we present gate replacement technique which reduces 43% of leakage current in 4×4 Wallace tree multiplier with full adders and the designers can add the sleep signal in non-critical paths there by not affecting the overall circuit delay, while significantly saving the overall leakage power.

### 6. REFERENCES

Agarwal, K., H. Deogun, D.Sylvester and K. Nowka, 2006. Power gating with multiple sleep modes. Proceedings of the 7th International Symposium on Quality Electronic Design, Mar. 27-29, IEEE Xplore Press, San Jose, CA., pp: 633-637. DOI: 10.1109/ISQED.2006.102

Assaderaghi, F., D. Sinitsk, S.A. Parke, J. Bokor and C. Hu *et al.*, 1997. Dynamic Threshold-voltage Mosfet (DTMOS) for ultra-low voltage VLSI. IEEE Trans. Elect. Devic, 44: 414-422. DOI: 10.1109/16.556151

Drakasan, C., A. Sheng and Brodersen, 1992. Low-power CMOS digital design. IEEE J. Solid State Circ., 27: 473-434. DOI: 10.1109/4.126534

Khandelwal, V. and A. Srivastava, 2004. Leakage control through fine-grained placement and sizing of sleep transistors. Proceedings of the IEEE/ACM International Conference Comput-Aided Design, Nov. 7-11, IEEE Xplore Press, pp: 533-536. DOI: 10.1109/ICCAD.2004.1382635

Khandelwal, V., A. Davoodi and A. Srivastava, 2005. Simultaneous V/sub t/ selection and assignment for leakage optimization. IEEE Trans. Very Large Scale Integr. Syst., 13: 762-765. DOI: 10.1109/TVLSI.2005.844304

Kuroda, T., T. Fujita, S. Mita, T. Nagamatsu and S. Yoshioka *et al.*, 1996. A 0.9-V, 150-MHz, 10-mW, 4 mm<sup>2</sup>, 2-D discrete cosine transform core processor with Variable Threshold-voltage (VT) scheme. IEE J. Solid-State Circ., 31: 1770-1779. DOI: 10.1109/JSSC.1996.542322

Lee, W., D. Kwong, D. Blaauw and D. Sylvester, 2003. Analysis and minimization techniques for total leakage considering gate oxide leakage. Proceedings of the 40th Annual Design Automation Conference, Jun. 2-6, IEEE Xplore Press, pp: 175-180. DOI: 10.1109/DAC.2003.1218934

Radhakrishnan, D., 2001. Low-voltage low-power CMOS full adder. IEEE Proc.Circ. Devic. Syst., 148: 19-24. DOI: 10.1049/ip-cds:20010170

Yuan, L. and G. Qu, 2006. A combined gate replacement and input vector control approach for leakage current reduction. IEEE Trans. Very Large Scale Integr. Syst., 14: 173-182. DOI: 10.1109/TVLSI.2005.863747