

A Discrete Event Modeling and Simulation of Wave Division Multiplexing Unidirectional Slotted Ring Metropolitan Area Network

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Abstract: Problem statement: The lack of uniformity in the choice of simulation platforms for optical WDM networks stands behind the difficulty of developing a common simulation environment. Correlating WDM unidirectional slotted ring network to Discrete Event Simulation (DES) encompassing event definition, time advancing mechanism and scheduler has yet to be developed. **Approach:** The study focused on the proposed and the development of an event based discrete simulator for the WDM unidirectional slotted ring network to facilitate the reuse of the protocol modules under a common simulation environment. The proposed network architecture implemented for the developed simulator employs a separate wavelength as the control information channel. This control information enabled the nodes to monitor their access to the transmission media. Each node was equipped with a tunable transmitter and fixed receiver for data communication. Access nodes were equipped with a fixed transmitter and fixed receiver for the control information exchange. The developed simulator had derived the use of dividing the wavelength into slots. Nodes used these slots to transmit fixed size packets. Slots can be reused by the access node after receiving packets by the deployment of the spatial reuse scheme, thus enhancing the bandwidth utilization. The developed simulator had derived the set of the parameters, events, performance metrics and other unique WDM simulator elements according to a detailed analysis of the base model. **Results:** The network delay and packet loss were investigated and compared to a benchmark of the modeled domain. Successful deployment of the developed simulator was proven by the generated results. **Conclusion:** Extensive performance analysis of WDM unidirectional slotted ring network can be deployed using the developed simulator with low computational overheads. Further enhancements were to extend the developed simulator for bidirectional slotted ring supporting fairness control and considering both uniform and non-uniform traffic.

Key words: Performance analysis strategies, optical networks, packet switching technique

INTRODUCTION

Optical Networks has enabled the deployment of applications such as video conferencing, remote medical assistant, TV streaming and distributed games, applications and databases. The common denominators of these applications are high bandwidth, low delay and function as the relaying backbone support to a multitude and heterogeneous network^[1]. In the wide spectrum of innovation created to optical components technology, switching has been made the core of this paper. Wave Division Multiplexing (WDM) has enabled single fibers to be optimized to its maximum potential. Thus, not imposing the need for multiple fibers to be installed and operated in parallel, resulting in significant cost savings. Optical WDM networks

exhibits supremacy mainly due to its low complexity and simple computational processing mechanisms.

In enhancing and developing the ring topology in WDM, performance analysis and its respective tools are evident. Analytical approaches have traditionally been widely utilized in the field of telecommunication networks, both for the design of new systems and for the forecast of the performance of existing networks. The migration to more sophisticated networks with increase trade-offs of complexity and capacity, the compulsory pre-requisite of assumptions in analytical methods has limited its adoption^[2]. Thus, the scalability and ability to capture the modeled system via simulation has been utilized extensively. Though there exist a wide myriad of simulation tools, there does not exist a detailed description and a developed General

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Purpose Language (GPL) DES for the WDM ring network. This study presents the development of a DES for WDM ring network and a comprehensive model development. The model can be adopted and customized for further analysis with ease.

The next discussion presents a detailed analysis of the related study. Subsequently, providing a comparative analysis of the available tools. This is followed by a discussion of the WDM ring network utilized as the basis of the DES. The details are then mapped into the proposed network model and segmented into the simulation components. The verification and validation of the developed simulator is deliberated prior to the study being concluded.

Related work: Simulation forms a substantial foundation in the performance analysis of optical networks. Several studies have been implemented for WDM rings encompassing both physical and media access layers. Most of these studies have been directed to specific problems as opposed to generic issues^[3]. Therefore, there exists a multitude of simulators for representing the performance of a wide spectrum of research areas in WDM optical networks. Optical WDM Network Simulator (OWNS) was designed to facilitate the study of switching and routing schemes in WDM networks. OWNS is an extension to the network simulator NS2. The extended NS2 simulator and OWNS were designed to analyze multi-protocols^[3,4].

Simulator for Optical Networks (SIMON) is an object-oriented event-driven simulation package implemented in C++ which incorporates optical device characteristics in the measurement of network-level blocking statistics. SIMON is suitable for studying the performance of large wavelength-routed optical networks, in which a call is set up in the network for a specific duration on a pre-determined light-path^[5,6].

Optical Packet Switch Simulator (oPASS), a simulation tool specifically designed for the evaluation of slotted Optical Packet Switching (OPS) switching architectures. oPASS is implemented in OMNET++, a general purpose event driven simulation framework. oPASS allows the evaluation of classical parameters in packet networks like packet loss probability and distribution of packet delay^[7].

Non-synchronized Optical Switch Simulator (NSOSS) is a simulator developed to simulate the behavior of a multi-port/multi-wavelength DWDM switching module and different buffering strategies^[8].

Automatically Switched Optical Networks Simulator (ASONS) extends the NS2 simulator with an additional simulation environment to enable experiments on automatically switched optical

networks. NS2 along with the ASONS extension module allows the modeling of ASON nodes and networks, configuring (i.e., switched) topologies and collecting statistics at the light-path and packet levels. The simulation environment was implemented as a set of distributed modules based on the G.8080 ITU-T recommendation^[9,10].

The lack of uniformity in the choice of simulation platforms for optical WDM networks stands behind the difficulty of developing a common simulation environment^[3]. These simulations packages allow the avoidance of reinventing the wheels of optical networks. However, there exist a significant correlation in the allowed level of programming and manipulation of provided frameworks. The need of such frameworks is the motivation behind this study to present a developed simulator for unidirectional slotted WDM ring network. The focus of the study is on the development of an event based discrete simulator for the optical unidirectional slotted ring network. The correlation of the developed simulator is generally done by first providing a detailed deliberation problem under study.

Unidirectional WDM slotted ring network: The critical design issues of unidirectional slotted ring, the respective architecture and the MAC protocol applied in the developed simulator environment requires detail analysis. In WDM ring optical networks, the node architecture and the protocol used to transmit data among them are the main issues related with the simulator's design. In this study, slotted ring has been selected as a platform for the developed simulators. Ring topologies have indeed been a solution for all-optical WDM networks, due to the successful ability of optical amplifiers to compensate insertion losses at intermediate nodes. Slotted rings allow slot synchronization even at extremely high data rates^[11]. Moreover, the ring topology permits the implementation of collision-free access protocols with no requirements for the usage of distributed algorithms or fixed access schemes as required by star topologies^[12]. The utilization of slotted ring eliminates channel and receiver collisions by the complementary deployment of Time Division Multiple Access (TDMA). Therefore achieving good throughput performance and provides fairness by allocating slots in a round-robin manner. Different protocols have been deployed to function with slotted rings. These protocols can be classified into protocols which are with and without channel inspection and those making use of separate control channels. The classification of slotted rings protocols influences the node architecture in terms

of the number of transmitters and receivers needed. Efforts for cost reduction encourages for networks to use simple nodes based on either Tunable Transmitter-Fixed Receiver (TT-FR) or (FT^W-FR), where W is the number of wavelengths. In this architecture, a number of N nodes can use any wavelength to transmit data while each node has its own wavelength to receive^[13-15]. The developed simulator in this study applies the TT-FR node architecture. Slotted ring networks avoid collision by enabling nodes to check the status of the slot (i.e., idle or busy). Two methods used to do this are:

- Adding the status information at the header of the data frame^[2,14-18] or
- Adding a separate Control Channel CC which holds the information of the slot status and of both source and destination information^[19,11,20-22]

The separate Control Channel (CC) wavelength method is used because it enables nodes to exchange control information at high line rates and eases the implementation of enhanced access protocols with fairness control and QoS support^[1]. The approval of standard IEEE 802.17 Resilient Packet Ring (RPR) serves as a testimony of the penetration of optical single-channel ring networks into high-performance packet-switched optical single-channel MANs^[1]. Channel inspection causes the need to defer the transmission of generated data. Therefore, leading to the use of Virtual Output Queues (VOQs) to store packets until the arrival of one or more available slots. The need to select the appropriate queue to transmit from has motivated a wide spectrum of algorithms which are mainly classified as priori and posteriori access strategies^[23]. In the priori access strategy a node selects the VOQ prior to inspecting the slot status. However, in the posteriori access strategy a node first checks the status of the slot and then selects the VOQ. The developed simulator in this study considers the posteriori access strategy. This strategy produces better channel utilization as compared to the priori strategy. Table 1, illustrates several posteriori VOQ selection algorithms.

From the described strategies in Table 1, the Longest Queue (LQ) selection strategy has been used as the core VOQ selection in the developed simulator. The LQ selection scheme provides better load balancing and fairness control as compared to the other selection schemes^[1,11,16,22,23].

Network model: The network model is presented in two main parts which are:

- The network architecture
- The utilized MAC protocol

Table 1: Posteriori VOQ selection strategies

Selection strategy	Description
Random selection	The VOQ from which a packet is to be transmitted is selected randomly according to a uniform distribution
Longest queue selection	The longest VOQ is chosen upon buffer contention
Round-robin selection	The VOQ is chosen in a round-robin fashion
Maximum hop selection	The packet in the respective VOQ associated with the maximum hop distance between source and destination node is selected when buffer contention arises
C-TDMA selection	Called also Channel-oriented TDMA (C-TDMA) scheme, each VOQ is allocated a certain slot within a TDMA frame of size W, where W denotes the number of wavelengths in the system

Network architecture: The unidirectional slotted ring consists of N nodes connected with a single optical fiber divided into Λ logical wavelength channels. Each channel is divided into fixed size timing slots. The timing slots respective boundaries are synchronized across all the channels. The slot duration equals to the transmission time of a fixed-size packet. Each node deploys N-1 VOQs, one for each destination node. The motivation behind this is to avoid the Head-Of-Line (HOL) blocking effect. Each VOQ holds up to B packets. Nodes also are equipped with one Tunable Transmitter and Fixed Receiver (TT-FR) connected with the data wavelengths. In addition, there is a Fixed Transmitter and Fixed Receiver (FT-FR) for the separate control information wavelength denoted as Control Channel (CC). Each node has its own drop wavelength (i.e., denoted as Node Home Channel) which is used to receive data which is directed to it. However a node can use any channel to transmit. Figure 1 shows an illustration of the applied model for $N = \Lambda = 4$ with a TT-FR node architecture. However, if $N > \Lambda$, then each wavelength is shared by several nodes for the purpose of receiving packets. Specifically, the destination nodes $j = i+n, \Lambda, n \in \{0,1,\dots, [N/\Lambda]-1\}$ share the same drop wavelength $i, i \in \{0,1,\dots,\Lambda\}$ ^[11,15,20,22]. Consequently, nodes sharing the same drop wavelength have to forward packets towards the destination node, resulting in multi-hopping. Slots are synchronized among the ring including the control channel slots which indicate the status of the next slots at the other channels. Thus the node is allowed to see one slot into the future. Figure 2 illustrates the concept of the CC in a wavelength with $\Lambda = 5$ channels.

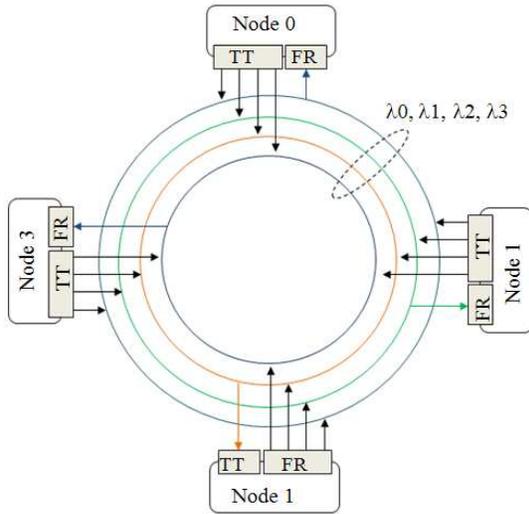


Fig. 1: Unidirectional ring network with TT-FR node architecture for $N = \Lambda = 4$

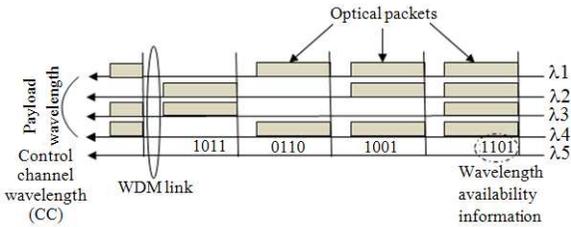


Fig. 2: The control channel wavelength provides the next slots status of the other correspond data wavelengths

Channels $\lambda_1, \lambda_2, \lambda_3$ and λ_4 are used for data packet transmission. Channel λ_5 is used as a Control Channel to indicate the control information in a slot which corresponds to the data (i.e., payload) wavelength occupancy in the next slot. The control information channel provides the slot status and the source/destination addresses. Figure 2 does not include the source/destination addresses to avoid the contention. In the destination node, the CC is inspected to check if the node has a packet to receive. If so, then the node takes the packet from the ring and resets the control slot information. The destination node may reuse the same channel used for receiving, to transmit its respective data. This process is known as destination stripping. With this destination stripping, wavelengths can be spatially reused by downstream nodes, leading to an increased network capacity.

Table 2: Default network parameters

Parameter	Default value
Network diameter	91.67 km
Number of nodes N	64
Number of wavelengths Λ	8
Link speed	2.5 Gb sec^{-1}
Propagation speed	$2.105 \text{ km sec}^{-1}$
Packet size	1500 bytes
Slot duration	$4.8 \mu \text{ sec}$
VOQ size	64 packets

MAC protocol: There is an additional wavelength channel for control information resulting in a total of $\Lambda+1$ channels in the network. The control channel plays an important role in the MAC protocol. This is because the nodes can access the wavelength by inspecting the information the Control Channel holds. Figure 2 shows the function of the Control Channel denoted as λ_5 . Each bit in the control channel λ_5 gives the status of the respective wavelengths. Nodes can know the availability of the next slot whether it is busy or empty. For example the status 1001 indicates that λ_1 and λ_4 are busy while λ_2 and λ_3 are available. If one or more slots are available then the node which has the access to the ring will transmit from the appropriate VOQ. The node selects the VOQ according to the posteriori strategy. Thus, the longest queue strategy is to check the $N-1$ VOQs in the node indexed from $j = 0$ to $j = N-1$ to determine the Longest Queue LQ (i.e., VOQ with the largest occupancy). The LQ with index $j=k$ is selected if the node home channel of the destination k is available. If there is more than one VOQ having the same length and the related wavelengths are available, the VOQ with the lowest index $j \in \{0, 1, \dots, N-1\}$ is selected. The scheduling of packets from the selected VOQ is done on a First in First Out (FIFO) basis. The busy slot status will be reset by the destination node after it receives the transmitted packet. The utilized network parameters are given in Table 2. The proposed simulator has derived and developed the unique features of the described WDM unidirectional slotted ring.

Proposed simulation model: The following discussion will realize the developed model through the deployment of a developed complementary simulator. The simulation components and the MAC protocol are mapped and reshaped in a form that can be interpreted in any General Purpose Language (GPL).

Assumptions: The developed simulation model derived two different groups of parameters. The first group includes parameters that serve as values reflecting the operating environment of the WDM. The second group of parameters serves as workload factors which assess

the functionality of the algorithm and queuing strategies. The following assumptions have been adopted to reflect a typical metro network:

- Nodes are equidistant to each other on the circumference of a ring with a diameter of 91.67 km
- Nodes are connected with $\Lambda = 8$ wavelength channels
- An additional wavelength channel is used as the CC to carry the control information. Thus, resulting in a total of $\Lambda = 9$ channels
- Each wavelength channel operates at a line rate of 2.5 Gb sec^{-1} (OC48) and the propagation speed on the optical fiber link is set to $2.105 \text{ km sec}^{-1}$
- The packet size is fixed at 1500 bytes, reflecting one of the dominant packet sizes in the Internet, as well as the maximum packet size. The maximum packet size is also known as the Maximum Transfer Unit (MTU) of Ethernet
- To get the corresponding slot size, the packet size is divided by the propagation speed. Thus, the slot duration becomes $4.8 \mu \text{ sec}$
- Each VOQ in the node has a length of 64 packets (i.e., $B = 64$)

The network traffic is generated using Bernoulli distribution^[2,11]. Bernoulli distribution was used to generate uniform traffic, where a given source node sends a generated packet to any of the remaining (N-1) nodes with an equal probability of $1/N-1$. The arrival rates applied are (0.0, 0.025, 0.05, 0.075, 0.1, 0.2, 0.4, 0.6, 0.8, 1.0). The average packet generation rate at each given node is σ . At a given node in each slot, a new packet is independently generated for each of the other N-1 nodes with a probability of $\sigma/(N-1)$. A newly generated packet is placed in the corresponding VOQ of the destination node or dropped if the respective VOQ is full. Subsequently increasing the packet loss. The fundamental and critical step in developing the proposed DES is the derivation of events. There are two methods formulated to derive an event. The first is a process or occurrence which changes the statistical composition of the WDM network. The second is the occurrences which are the direct propagation of the execution of an existing event. The failure to derive the appropriate events will have a direct implication on the developed simulator's correctness.

Simulation events: The derivation of events is based on a detailed examination of the algorithm and the respective statistical changes observed. The mapping of the observations to the needed simulator components

has lead to three main events. These events were packet arrival, transmit packet and packet receive. Subsequent analysis of these events has led to the formulation of sub-events such as inspecting the control channel information, updating this information and finding the longest queue. The functions of the defined events are shown in Table 3. Figure 3 shows the event flow diagram for the WDM unidirectional slotted ring per-packet processing. The simulation has been developed to capture the essence of this processing. The distinct difference between an application and simulation is the scheduler function^[3]. The scheduler in the developed simulator ensures that the activation of the derived events in Table 3 is invoked based on their respective activation time.

Scheduler: Scheduler is the main controller for any simulation. It maintains the list of events to be executed according to their respective time stamps and simulation clock. In the developed simulator, the control channel CC played an important role in the design of the scheduler.

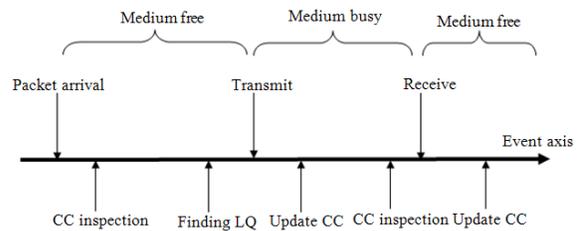


Fig. 3: Event flow diagram for a single packet

Table 3: Derived events and functionalities

Event	Function
Packet arrival	Comprises of the generation of a new packet and assigning a random destination to it. The destination can be any one of the other N-1 nodes. The generated packet is queued at the destination respective VOQ. If the queue is full, the packet will be dropped.
CC inspection	Checks the control channel information. This information is utilized for the controlling of the scheduling process for the other events
Queue selection	To determine the appropriate LQ to transmit from based on the available slots.
Transmit packet	Includes transmitting the packet from the selected longest queue, changing the slot status (i.e., updating the CC information) and decreasing the queue size one
Packet receive	Inspecting the control channel information related to the current node home channel. The purpose is to check if it contains a packet directed to it. After the node has received the packet, it updates the slot to make it free. the node can reuse the same channel to transmit its respective data (i.e., destination stripping)

This is because the simulation clock was computed in slots and the control channel governs the events at each slot time. The developed simulator has programmed arrival event to take place first before any of the other events. Therefore, in order to enforce this sequencing, the first packet arrival event is scheduled at slot-time = 0. Subsequent arrival events are subject to the principle that a new packet is independently generated for each of the other N-1 nodes with a probability of $\sigma/(N-1)$. The control channel then governs the execution of the simulation events as follows:

- Execution of the arrival event. Generate a packet deploying the Bernoulli distribution and assigning a random destination to it. The generated packet is then placed in the corresponding VOQ of the destination node or dropped if the involved VOQ is full
- Execution of the CC inspection event to check the slot status and to determine the next event
 - If the slot status equals 1 and the channel is related to the node as its home channel, then the destination name associated with the slot status in the control slot is checked. If the packet held by the home channel is directed to the current node, then the receive event is executed
 - If the slot status equals 0, then the queue selection event is executed
- In finding the longest queue event, the longest queue is selected and recorded in the related CC information to be used in the next event, which is the transmit event. If no queue is found to transmit from, the control to the slot and the wavelength is given to the next node in the ring
- If the event is transmit, the corresponding queue size is reduced by one and the important statistical information is updated
- If the event is a receive event, the packet is removed from the corresponding channel and the control channel resets the related information

Simulation algorithm: The formulation of the execution of the events in an algorithmic format is developed to enable clarity. Figure 4 presents the developed algorithm for the simulation. The major components are as follows:

- Initialization of:
 - Simulation clock
 - Networks parameters, such as the number of nodes and channels and mean arrival rate

- Passive objects, like VOQs and node home channel
- Initial performance metrics values
- State times of the respective events
- Execution of arrival of packets at each node according the σ probability
- Execution of the following events until the convergence of the termination of the simulation is fulfilled (e.g., 10^6 slots or more):
 - Packet arrival and queuing
 - Inspecting the control channel-to determine the next event as follows:
 - The transmit event will be executed if there is a tie between the available slot and the longest queue LQ by executing the find LQ event. The selected LQ size has to be reduced by one
 - Receive packet is an event activated when the node inspects the control information related to its home channel and finds a packet directed to it. The performance parameters for analyses are obtained during transmit and receive events. Examples of the pertinent performance metrics are number of packets transmitted, number of packets received and packet delay

Performance metrics: In this study, two performance measures are considered which are, the relative packet loss and the mean packet delay. These metrics are defined as follows:

- The Relative Packet Loss (RPL) in the network is defined as the ratio of the total number of dropped packets (TDP) to the total number of generated packets (TGP) in the network (i.e., Eq. 1):

$$RPL = TDP / TGP \quad (1)$$

- The Mean Packet Delay (MPD) in the network is defined as the time period elapsed from the generation of a packet to the time the packet has completed its processing (i.e., Eq. 2)

Verification and validation: The validation of the developed DES is achieved by comparing and analyzing the acquired results against benchmark results. The evaluation is done to ensure that the developed simulator indeed serves as a worthy performance analysis tool. It is worth mentioning here that using different simulators to evaluate the same model may present the same results with a deviation ratio.

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1. Initialization of the simulator
  I. Initialize the network parameters: no. of Nodes N←64, no. of channels Λ←8, no. of control channel CC←1,
     max queue size mQsize←64, simulation clock (slot time) st←0, No. of packet transmitted npt←0, total
     packet loss tpl←0, total packet received tpr←0, total delay td←0, delay duration time ddt←0, packet receive
     time prt←0, mean packet delay mpd←0, relative packet loss rpl←0, total packet arrive←0
  II. For all nodes do the following
      a) Determine the node home channel nhc, nhc[node n]=n % Λ
      b) For all N - 1 destination VOQs dn do the following
          i. Node[dn][ mQsize] ← 0
          ii. Index[dn] ← 0
      End-for
      c) Initialize the control channel information
          i. For each control slot cs, cs<= Λ do
              Slot status, sst← 0, Source node, sn← 0, Destination node, den← 0,
              Packet arrival time, pat← 0
          End-for
      End-for
  III. Define the packet generation rate array,
      pgr[10] ← [0.0,0.025,0.05,0.075,0.1,0.2,0.4,0.6,0.8,1.0]
2. For each new experiment E, E<=10 do the following
3. While ( st <106) do the following
  a) Arrival rate for the current experiment ← pgr[E]
  b) For each node n do the following
      • If Bernoulli distribution condition is satisfied, then
          • Generate a packet, assign a random destination dn
          If index[dn] < max queue size then index[dn]++, tpa++
          else, drop the packet, tpl++
          Move to the next node
          • Inspect the control slot information
          1) If cs [nhc[current node n]].slot status = 1 and cs[nhc[current node n]].destination= n,
             execute receive event
             Calculate the delay duration time,
             prt←st, ddt←prt-cs[nhc[n]].pat
             Increase total delay, td←td+ddt
             reset the control information
             cs[nhc[n]].sst ← 0, cs[nhc[n]].sn ← 0, cs[nhc[n]].den ← 0, cs[nhc[n]].pat ← 0
             increase no of packet received, tpr++
          2) If only one slot is available, check if the related VOQ has a packet to send
             A) Update the control information:
                 cs[nhc[dn]].sst ← 1, cs[nhc[dn]].sn ← n, cs[nhc[dn]].den ←
                 VOQ.id, cs[nhc[dn]].pat ← st
             Index[dn]← index[dn] - 1, npt++
             B) else move to the next node
             o If more than one slot are available, and related queues have packets
               to send, then select the longest queue
               Repeat step 3. b.ii.2.A
             If the queues have the same length,
               Select the queue with the lowest index
               Repeat step 3. b.ii.2.A
      c) If st>=106 (transit period)
          i. Calculate results,
             mpd← (td/tpr)/N,
             rpl←tpl/tpa
  end while;
end for E

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Fig. 4: The proposed simulator algorithm

Furthermore, different simulation strategies may cause different propagation delays and different results of rescheduling^[23]. Many factors stand behind the results inequality. For instance, a constrained-random test may not give the same results when run on different simulators, or even on different versions of the same tool^[24]. The particular details and architectural techniques considered and the compiler choice has a significant and non-uniform impact on predicted performance trends. Furthermore, the instruction cache model is the most critical element for an accurate simulation of compute-intensive benchmarks in addition to the fidelity of the memory system model. There is also a significant impact on the simulation results acquired^[25]. As an example of the architecture

and the interior hardware circuits' structure impact, a simple three input AND gate produced a 23% difference in the fault coverage between two simulators^[26]. Furthermore, an Exclusive NOR gate yielded fault simulator differences by as much as 6%. Likewise, different manufacturers of Electrostatic Discharge Simulators (ESD) designed to meet the requirements of IEC801.2 produce different results^[27]. When evaluating the pulse in the time domain they appear to meet the requirements when the traditional rise-time definition is used. Some simulators exhibit high frequency components, nonlinear rise from 10-90% points^[28].

As mentioned before, this study developed a WDM DES based on the C programming language under

Microsoft Visual C++ environment. The provided random number generator has a significant impact on the acquired results by the developed simulator. However, the benchmark (i.e., used to evaluate the developed simulator) uses the OMNET++ simulator and its respective random number generator. The achieved results from the developed simulator in this study are analogous to the benchmark results with an acceptable deviation.

RESULTS AND DISCUSSION

The developed simulator has deployed the Bernoulli distribution which generates a uniform traffic with the probability $\sigma/(N-1)$. Destinations are selected randomly and associated with each generated packet. The packets are subsequently forwarded to the related VOQ with available space. The simulation was run for 10^6 slots. The number of running slots in the simulation is chosen to ensure the ability of generating a steady state average of the expected results. Different arrival rates have been tested to provide different workload in network. The simulator is evaluated in terms of the relative packet loss and mean packet delay in the network. These measures and the steady state transaction times are measured after a transient period of 10^5 running slots.

The results were plotted in relation with the mean arrival rate computed from this distribution. For the network delay, Figure 5 shows the developed DES acquired delay as compared to the benchmark. The developed simulator has successfully regenerated the benchmark work with an average deviation ratio of 11.5%. The developed simulator has significantly represented the pattern of the WDM operations. Figure 6 shows the tested packet delay for different number of nodes $N = 32$ and 64 respectively. It shows that as the number of nodes is increased, a higher average delay is recorded. This experiment proves the theoretical assumption of WDM behavior. As the load increases, the slots are utilized higher causing them to be constantly busy. Thus, delaying the transmission process of the queued packets. The slots constant consumption and the high load in the network leading to the node's queues to be constantly occupied at the highest point. Subsequently, leading to the packet loss in the network. Figure 7 shows that the acquired results for the packet loss from the developed simulator has captured the benchmark results with a deviation of 4.3%. Figure 8 shows the mean packet loss for different numbers of nodes, $N = 32$ and 64 respectively. The results replicate the actual behaviour that the number of packet loss is highly affected at higher

loads. This is due to the slots occupancy and full utilization of the VOQs.

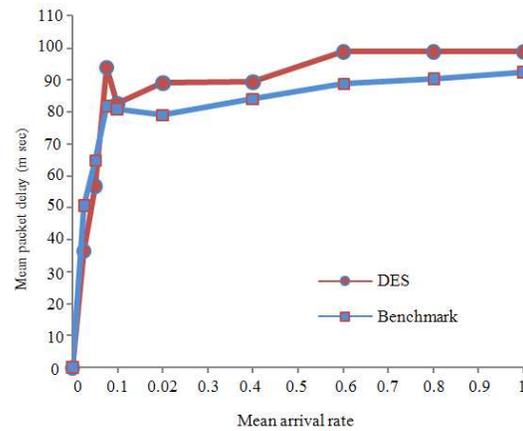


Fig. 5: Mean packet delay for the network under Bernoulli traffic

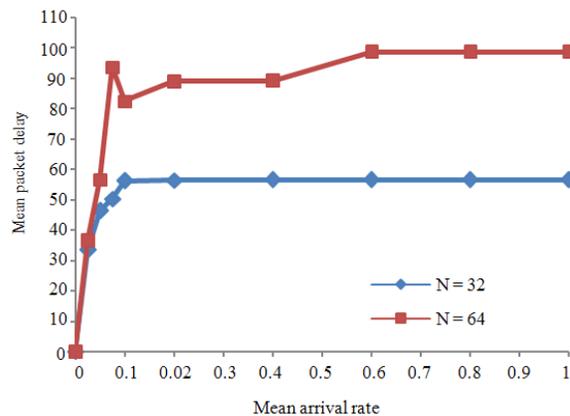


Fig. 6: Mean packet delay for the network under Bernoulli traffic with N = 32 and 64

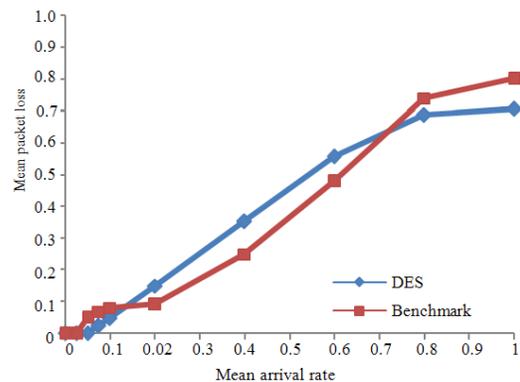


Fig. 7: Mean packet loss for the network under Bernoulli traffic

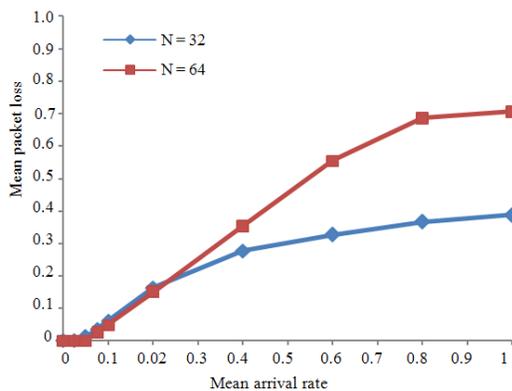


Fig. 8: Mean packet loss for the network under Bernoulli traffic for N = 32 and 64

CONCLUSION

In this study, a detailed description is provided for a simulator developed to examine and validate the performance of the WDM unidirectional slotted ring network. The environment provides clearly delineated components to model each aspects of the system. The simulation system is developed using a GPL which enables scalability and deployment convince. The considered performance metrics were the mean packet delay and the relative packet loss. The acquired results from the developed simulator are analogous to the results obtained in the benchmark. However, the key advantage is the alternative performance analysis tool with low computational overheads. The simulator is in progress of being embedded with bidirectional slotted ring as future research efforts.

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