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New Development Design of Low Current Measurement with Noise Reduction for High-Resolution System

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Abstract: The treatment of inoperable cancers in the therapy terminal in Lanzhou-China, which is located at the Institute of Modern Physics (IMP), permits to work on the actual front-end readout. The availability of detailed noise spectral density characteristics for the OPA amplifier helps to develop the noise error analysis for high-resolution. This work focused on the noise model of the detector-preamplifier, which presents the low noise circuit schematic of the Transimpedance (TIA). Considering the parasitical influences, we develop a new approach to detect the weak signals based on resonant frequency, $1/\sqrt{L_1}$ (C_1+C_{GS}). In addition, the system eliminates leakage current in the reset switch and reduces the charge injection occur from the switches in the Gated Integrator (GI) and the configuration switch is made especially with two transmission gates switches, in series, with a grounded MOS switch, attached to the node between the two transmission gates switches and the linearity almost good.

Keywords: Photodiode, Transimpedance, Noise, Charge Injection Leakage Current, Transmission Gates

Introduction

The optical receiver front-end plays an important role in transmission systems and the sensitivity of the receiver usually suffer by the impact of different noise factors. In the recent years, since 2006 at Institute of Modern Physics, Lanzhou, beams of heavy-charged particles like carbon ions have encouraged the research of measurement structures and these beams have been used to the treatment of inoperable tumors with different detector arrays of silicon strip detectors (Zhou *et al*., 2012). Beams used to the treatment in many cases always have very low currents less than a pico-ampere. Construct low beam current measurements disturb a lot and suffer from poor accuracy from the noise factors. Thus, there must be a compromise between the precision and bandwidth of the measurement system to accurately measure the beam current. Several systems previously studied for measurement of currents in this order of magnitude are limited in their bandwidth and gain (Auzelyte *et al*., 2006). The capacity to extract particle parameters directly at room temperature with high-resolution could make these detectors a good choice for micro instrument, furthermore, the detectors will widely be applied in biomedicine, industry, antiterrorism, astrophysics, physic etc. (Auzelyte *et al*., 2006; Kong *et al*., 2010).

Since semiconductor makes the detectors, the design of front-end readout circuit is useful to detect the low signals (Zhang and Wu, 2011; Beikahmadi and Mirabbasi, 2011). This paper will present a description designed of a low current measurement circuit for the beam current control system. Firstly, in this paper, we will describe a front-end readout circuit necessary to detect the weak signals of detectors by reducing a noise gate. Secondly, we will develop the configuration switch of gated integrator based on reduction leakage current, charge injection and the noise prevention.

Low Current Measurement Circuit

The Block diagram Fig.1, shows the heavy ion beam current control system. The accurate low current measurement circuit scheme in nowadays consists of a novel technique I/V Converter and a new approach of Gated Integrator which avoid the parasitical influences. The current signal from the detector, is converted into a voltage signal through a I/V Converter, the output of which is integrated by the GI to measure the charge of the beam (Zhou *et al*., 2012; Kong *et al*., 2010; Redondo *et al*., 2007). Outputs of I/V Converter and Gated integrator are acquired by a data acquisition system based on PXI. The local computer processed the signals.

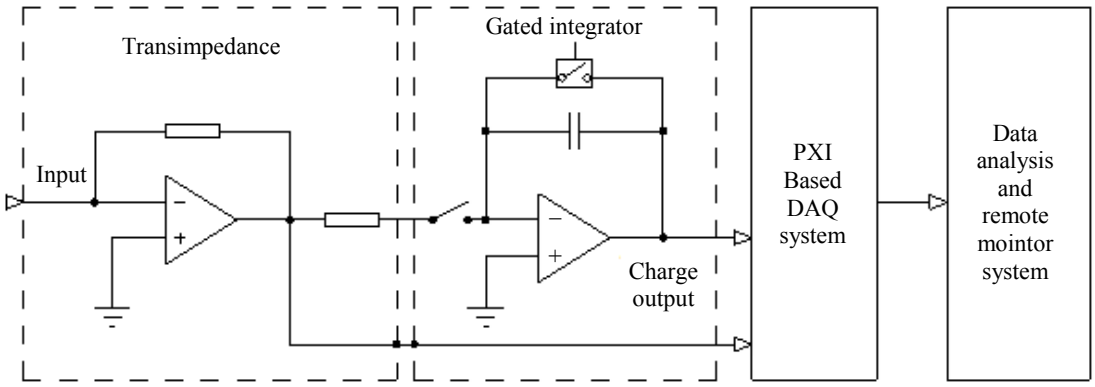


Fig. 1: Block diagram to read the heavy ion beam control system

The different from conventional Preamplifier and semi Gaussian shaping amplifier output, which is integrated on the feedback capacitor C_f, the two separated parts of new circuit prevent against many parasitical influences such as: noise sources of the transimpedance, charge injection of reset switches, leakage current of the feedback capacitor and the noise during a transient voltage excursion.

The Design of the Transimpedance with Low Noise

Noise Analysis of the Transimpedance

Because of detailed noise spectral density characteristics for the OPA amplifier, which allows an accurate noise error analysis, we can take into consideration parasitical influences shown in Fig. 2. The output voltage of the Transimpedance can be described by Equation (1):

$$U_o = -I_S R_f - \left(I_{na} - I_b - I_{nR}\right)R_f + \left(1+\frac{R_f}{R_S}\right)U_{na} = -I_S R_f + U_n \quad (1)$$

$$U_n = -\left(I_{na} - I_b - I_{nR}\right)R_f + \left(1+\frac{R_f}{R_S}\right)U_{na} \quad (2)$$

where, I_b is the input bias current of the amplifier, I_{na} is the instantaneous value of the input noise current of the amplifier, I_{nR} is instantaneous value of thermal noise current of the scaling resistor and U_{na} is the instantaneous value of input noise voltage of the amplifier (Levinzon, 2005; Wembe *et al*., 2014).

The ideal solution is to cancel out or reduce completely to zero the effect of noise equation presented in the Equation 2. The improvement of the noise should not affect negatively on the feedback circuit bandwidth, Fig. 2, when a large R_F is required due to small input currents into the TIA with, the inherence capacitance of the detector C_D, given by (Graeme, 1996):

$$BW_{TIA} \approx \sqrt{\frac{GBW}{2\pi R_F C_D}} \quad (3)$$

Structure of the Series LC Tank TIA

Considering the Equation (1), a low noise current, a low noise voltage and a low bias current are needed to minimize the noise figure of the transimpedance preamplifier. In order to address these issues, we develop a new structure of transimpedance preamplifier whose block diagram is presented in Fig. 3.

Noise Suppression Technique

In a conventional TIA with a feedback resistor as shown in Fig. 2, using JFET operational amplifier, there are two main noise sources; thermal noise from the feedback resistor and gate noise from operational amplifier. Moreover, from the two noise, the thermal noise of the feedback resistor adds only a small contribution to the input referred current noise in the high frequency area because the thermal noise is commonly a white noise and constant versus frequency. The current thermal noise Power Spectral Density (PSD) is inversely proportional to the resistance, which is quite small when a large feedback resistor is used to amplify a very small input current. The gate noise is composed by noise current and noise voltage. The noise current, $\overline{i_n^2}$ is defined by the induced thermal noise from the drain, $\overline{i_{n1}^2}$ and the shot noise from the channel, $\overline{i_{n2}^2}$ and the noise voltage, $\overline{e_n^2}$ is defined by the thermal noise in the channel, $\overline{e_{n1}^2}$ and the drain current flicker noise, $\overline{e_{n2}^2}$ expressed by (Sergio, 2015):

$$\overline{i_n^2} = \overline{i_{n1}^2} + \overline{i_{n2}^2}, \overline{e_n^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} \quad (4)$$

$$\overline{i_{n1}^2}=\left(\frac{2\pi fC_{GS}}{g_m}\right)^2\left(4kT\frac{2}{3}g_m+K\frac{I_D^a}{f}\right)\Delta f,\overline{i_{n2}^2}=2qI_G\Delta f \quad (4a)$$

$$\overline{e_{n1}^2}=4kT\left(\frac{2}{3g_m}\right)\Delta f,\overline{e_{n2}^2}=4kT\left(K\frac{I_D^a g_m^{-2}}{f}\right)\Delta f \quad (4b)$$

where, g_m is the transconductance; I_D is the dc drain current; k is the Boltzmann constant, T is the absolute temperature; I_G is the gate leakage current K and a are appropriate device constants and C_{GS} is the gate to source capacitance.

Compare these noise sources either current or voltage noise apply for high frequency and wideband applications; the induced drain noise is dominant because the noise is a quadratic function of frequency, as presented in Equation (4a). Generally, the noise rapidly increases at frequencies beyond the gigahertz range. In order to reduce noise from the first-stage transistor of TIA, a series LC circuit, which has theoretically zero impedance at the resonant frequency, is implemented as shown in Fig. 3 (a). The inductor, L_1 in series with the prevent capacitance, C_1 and the gate capacitance, C_{GS} forms a series LC circuit. Then the impedance, Z_{in} is defined:

$$Z_{in}=r+j\omega L_1+\frac{1}{j\omega\left(C_1+C_{GS}\right)} \quad (5)$$

where, r is an intrinsic resistance of the inductor, C_{GS} is the gate capacitance and C_1 is the prevent capacitance. Although this parasitic resistance reduces the quality factor, which determines the deepness of the noise reduction at the resonant frequency, the series LC circuit reduces the gate noise contribution to the input referred current noise at the resonant frequency, which should be set at the 3 dB bandwidth of the TIA. The input noise density function in Fig. 6 presents the effect of the noise suppression technique at the different target frequencies versus different inductors. The target frequency applies for the noise suppression technique is calculated by $1/\sqrt{L_1(C_1+C_{GS})}$ which is the resonant frequency of the series LC series.

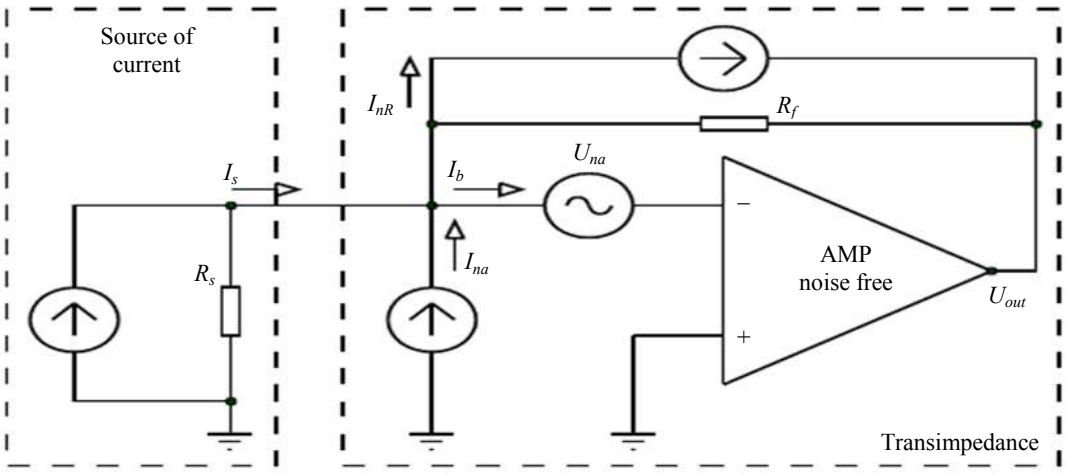
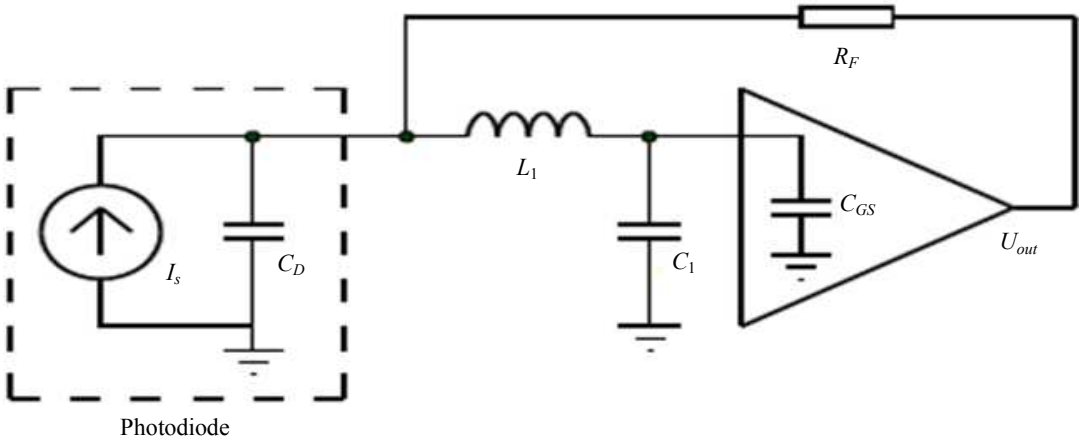
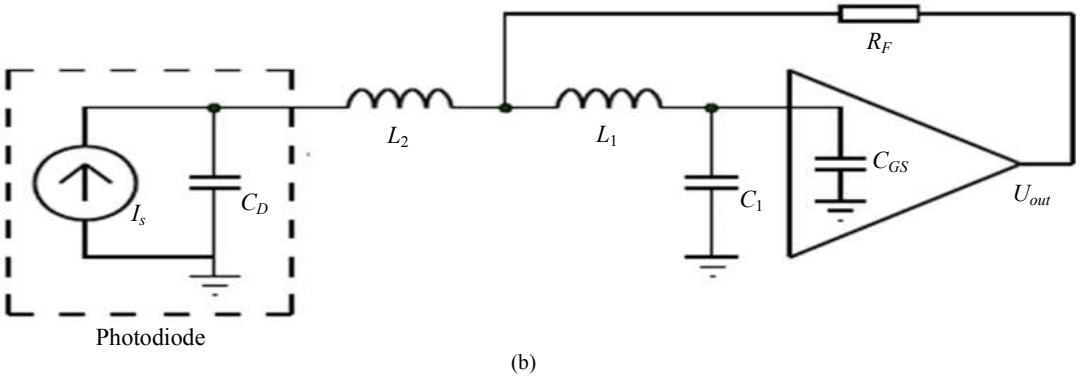


Fig. 2: Transimpedance circuit with main error sources



(a)



(b)

Fig. 3: Structure of the transimpedance amplifier for noise suppression through Z_{INP} (a) instable case (b) Stable case

However, the added inductor L_1 and capacitor C_1 at the input node forms a parallel *LC* circuit with the inherent capacitances of the input of the TIA and of the radiation detector, C_{GS} and C_D respectively can provoke instability. To characterize the system stability since Z_{INP} and R_F help to define a feedback factor β, the impedance Z_{INP} of the Fig. 4a, is expressed by:

$$Z_{INP} = \frac{\left(1+p^2L_1\left(C_1+C_{GS}\right)\right)}{p\left(C_1+C_{GS}+C_D\right)\left(1+p^2\frac{L_1\left(C_1+C_{GS}\right)C_D}{C_1+C_{GS}+C_D}\right)} \tag{6}$$

The analysis of this Equation (6), can present many poles on the open loop, which conducts in an instability situation. In order to eliminate these poles, we add another inductor L_2, which forms another series *LC* circuit with C_D as presented in Fig. 4b. The impedance Z_{INP}, becomes:

$$Z_{INP} = \frac{\left(1+p^2L_1\left(C_1+C_{GS}\right)\right)\left(1+p^2L_2C_D\right)}{p\left(C_1+C_{GS}+C_D\right)\left(1+p^2\frac{\left(L_1+L_2\right)\left(C_1+C_{GS}\right)C_D}{C_1+C_{GS}+C_D}\right)} \tag{7}$$

The Equation (7) is simplified when a chosen value L_2, satisfies $T = L_1(C_1+C_{GS}) = L_2C_D$, then:

$$Z_{INP} = \frac{\left(1+p^2T\right)}{p\left(C_1+C_{GS}+C_D\right)} \tag{8}$$

The impedance Z_{INP} in Equation (8) is formed by two zeros and no pole, if we choose carefully either L_2 or C_1 in accordance with *3 dB* bandwidth of the TIA.

With the stability case, for high-resolution applications, an equivalent noise analysis was performed with all noise sources; thermal noise from the feedback resistor, e_f and the added inductor, e_Z and induced gate noise, i_n from the TIA as presented in Fig. 5. The output noise PSD of the TIA design can be analytically derived by superpositioning each noise source. From the beginning, e_f and e_Z are converted to the output noise as the node at the detector side, which is generally assumed an open with high detector resistance. The voltage noise PSDs are expressed respectively:

$$\overline{e_f^2} = \int 4kTR_F df \tag{9}$$

$$\overline{e_{Zin}^2} = \int 4kTZ_{in} df \tag{10}$$

$$\overline{e_{ni}^2} = \overline{i_n^2}\left(Z_{in}\right)^2 \tag{11}$$

where, Z_{in} consists of the inductor, L_1 and the gate capacitance, C_{GS} of the first-stage transistor with a parasitic resistance, *r* in Equation (5). This series *LC* component is a main factor for the technique to reduce the input current noise at the resonant frequency while L_2 noise is not dominant for total output noise because the thermal noise from the intrinsic resistance of an inductor is negligible in general. The induced gate noise defined in Equation (11) affects the output voltage noise through the impedance, Z_{in}:

Finally, the total input current noise $\overline{i_{Tot}^2}$ in Equation (12) can be defined by the total input voltage, which is a sum of all voltage noise sources divided by the transimpedance gain, R_F, given by:

$$\begin{aligned}\overline{i_{Tot}^2} &= \frac{1}{R_F^2}\left(\overline{e_f^2}+\overline{e_{Zin}^2}+\overline{e_n^2}+\overline{e_{ni}^2}\right)\\ &= \int\left[\begin{array}{l}\frac{4kT}{R_F}+\frac{4kTZ_{in}}{R_F^2}+\frac{4kT}{R_F^2}\left(\frac{2}{3g_m}+K\frac{I_D^a g_m^{-2}}{f}\right)\\ +4kT\delta g_m\left(\frac{2\pi fC_{GS}}{g_m}+K\frac{I_D^a}{f}\right)^2\frac{Z_{in}^2}{R_F^2}\end{array}\right]df\\ &= \int\left[\frac{4kT}{R_F}+\frac{4kT}{R_F^2}\left(\frac{2}{3g_m}\right)\right]df\end{aligned} \tag{12}$$

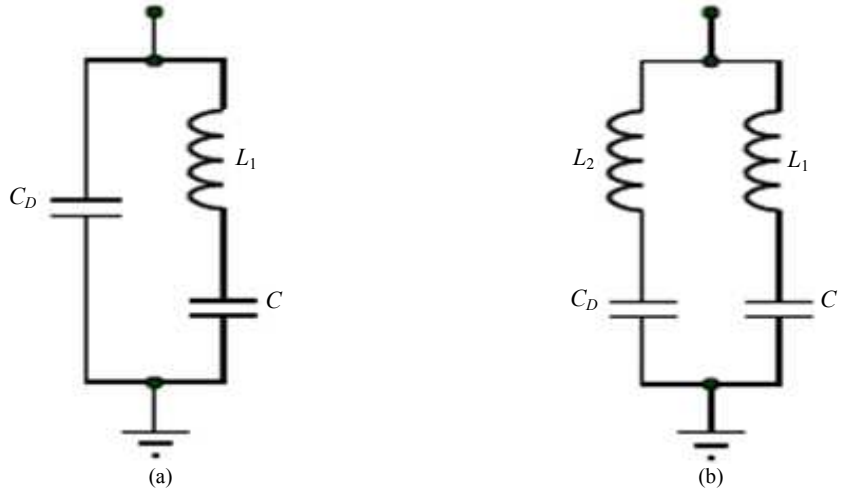


Fig. 4: The impedance ZINP (a) instable case (b) Stable case and control bandwidth.

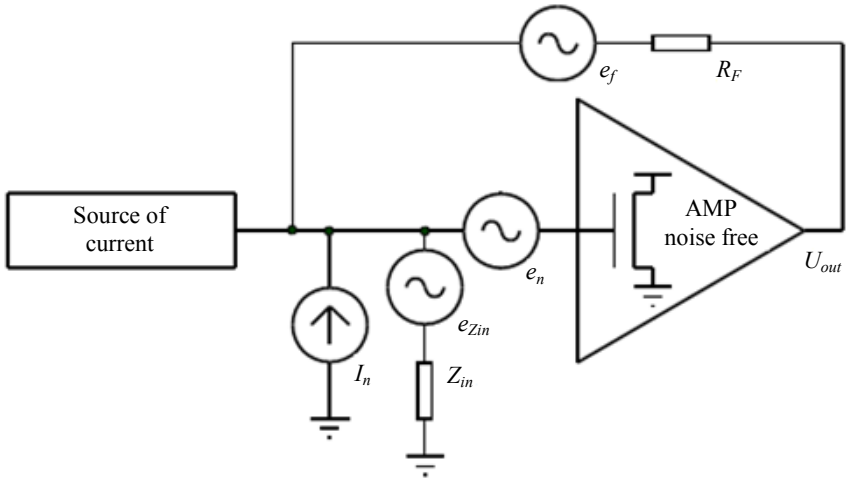


Fig. 5: The main noise sources contributing to input for new TIA

At the resonant frequency of Z_{in}, the impedance becomes almost zero if the parasitic resistor r is negligible and the fourth term of Equation (12) is canceled out. The real impact helps to reduce the rapidly increasing induced gate noise as the frequency increases as discussed earlier. The input noise density in Fig. 6, presents the effect of the noise suppression technique. Moreover, in the Fig. 6 (a), we see the noise effect versus inductors and frequencies, which shows the impact of the inductor on the bandwidth. The Fig. 6 (b) shows the conventional TIA noise aspect; while Fig. 6(c) presents the deepness noise suppression provoke by the series LC circuit. Furthermore, the inductor has the impact on the high frequency and wideband applications, when the close-loop transfer functions, shown in Fig. 7, were measured with different inductors. The TIA successfully increases the bandwidth through the inductive peaking. Note that larger inductor can make the system unstable due to circuit imbalance.

Table 1: Main parameters of TIA

Parameter	Value
C_D	$10pF$
C_{GS}	$1fF$
C_1	$1pF$
R_D	$100M\Omega$
R_F	$100k\Omega$
L_1	$1nH$
R	0-5Ω
L_2	$100nH$

In comparison to the baseline TIA, the overall bandwidth is enhanced while maintaining the system stability. The intrinsic capacitance of the detectors reduces the bandwidth and gain as shown in Fig. 8.

After targeting the particle with low noise preamplifier system with the specifications in the Table 1, we can now treat the signal through the gated integrator.

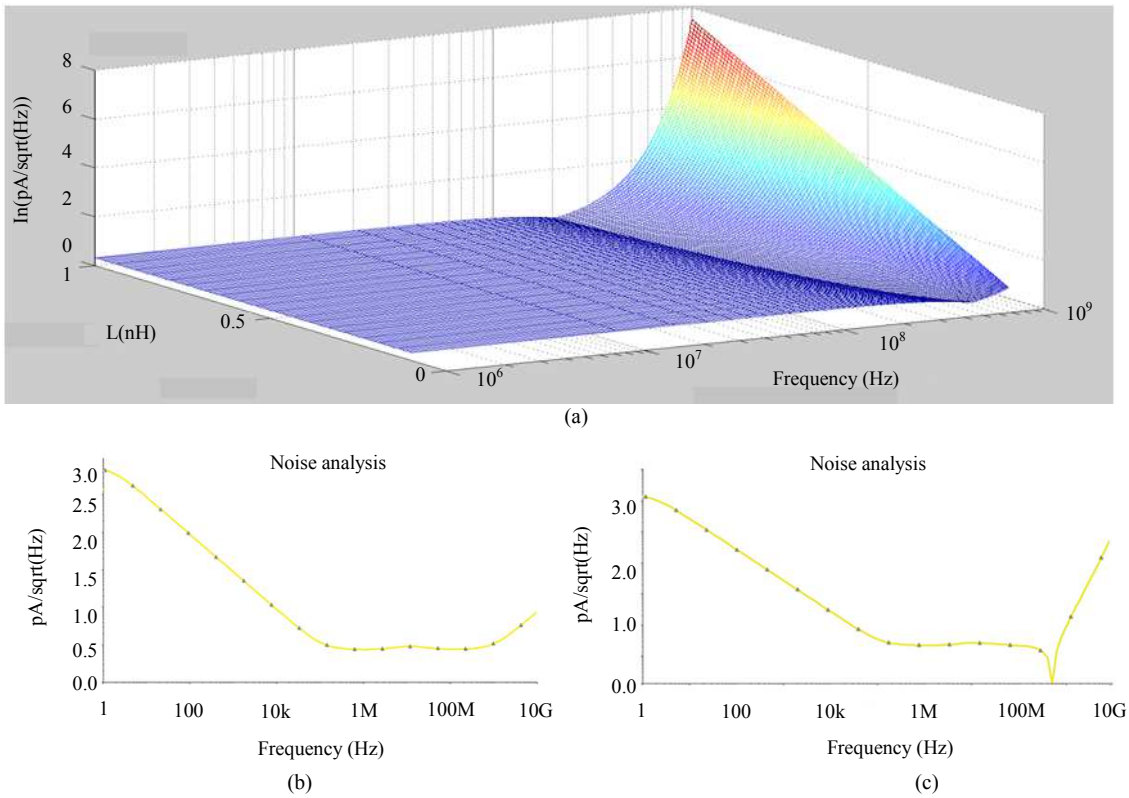


Fig. 6: Gate induced input current noise simulation of the TIA

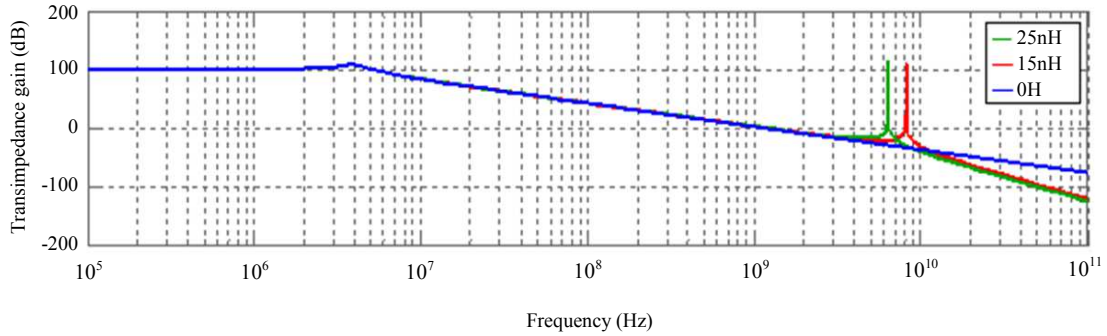


Fig. 7: Measured frequency responses with different inductors

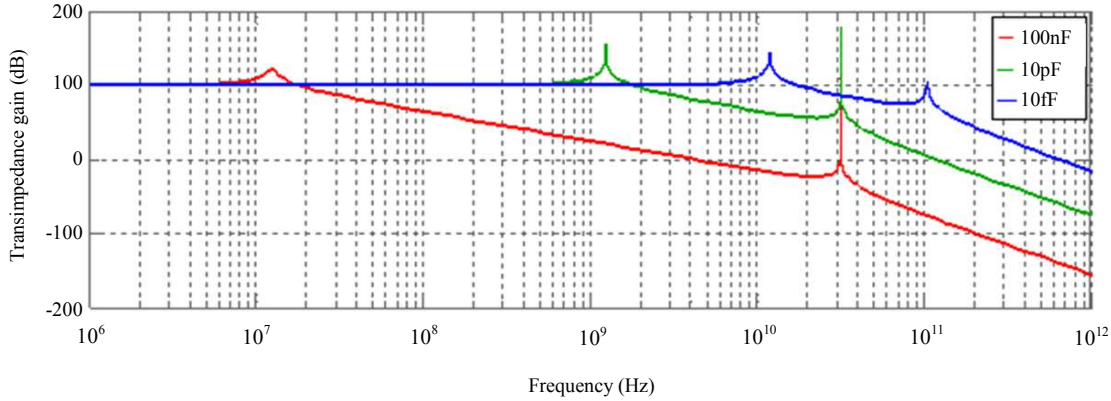


Fig. 8: Measured frequency responses with different input capacitance

The Structure of the New-Gated Integrator

A gated integrator is built to receive and integrate low and fast signals with time scales between 1*0ps to* 1*00μs*. Moreover, a gated integrator is used to amplify and integrate the signal that is present a moment the gate is open, without noise and any disturbances that may be present at other times. The gated integrator is ideally a capacitive transimpedance amplifier except the gated switch, so it also performs as a filter. In our measurement system to receive the entire charge of the beam, the output of the transimpedance is connected into the GI, the schematic indicated by the second dotted line in Fig. 1. The input signal voltage U_i is converted into current through the resistor and integrated by the feedback capacitor C. The output voltage U_{out} is obtained by:

$$U_{out} = \frac{1}{RC}\int_0^T U_i(t)\,dt + U_0 \tag{13}$$

where, U_i is the input voltage, proportional to the current from the transimpedance, U_{out} is the GI output voltage, which represents the total charge of the beam for a given duration T and U_0 is the initial voltage in the feedback capacitor of the GI. The leakage current suppression techniques and charge injection compensation were implemented in the GI section. The GI circuitry is composed of switches, operational amplifier and capacitors. The non-ideal switch and amplifier will introduce additional noise and fixed pattern (J.G. Graeme, *Photodiode Amplifiers: OP AMP Solutions*. McGraw, 19 Sergio, 2015). The aim of the design is trying to understand the issues and take appropriate strategies to suppress them such that the performance of the circuitry is not overshadowed.

Configuration Switch to Prevent Leakage Current and Charge Injection

When it is a time for integration of the gated integrator, the effect reset switch has to be kept off. However, the effect of leakage current in the GI reset switch will induce errors to the output in the long time of these states. This problem can be resolved by using the configuration switch shown in Fig. 9 to replace single reset switch.

A MOS as a switch is used to conduct voltage or current from one end to another. An ideal switch has the characteristics of zero resistance when it is ON, infinite resistance when it is OFF and no delay when it is turned ON or OFF. A real MOS switch however, has turn-on non-zero channel resistance, turn-off leakage current, parasitic capacitances and threshold voltage. If the body and source are at the same potential, the drain to source current of a MOS transistor in the deep sub-threshold region of operation is expressed by:

$$I_D = KI_{DO}\cdot\exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$
$$I_{DO} = \mu_n C_{OX}(\eta-1)V_T^2 \tag{14}$$

where, I_D is the drain to source current of the transistor MOS, K is the aspect ratio of the transistor, I_{DO} is the saturation current, V_{GS} is the gate to source voltage, V_{th} is the threshold voltage of a MOSFET, V_T is the thermal voltage, V_{DS} is the drain to source voltage, μ_n is the carrier mobility, C_{OX} is the gate oxide capacitance and η is the sub-threshold slope factor (Riboldi *et al*., 2010; Sergio, 2015; Ueno *et al*., 2010; McGraw-Hill Education, 2017).

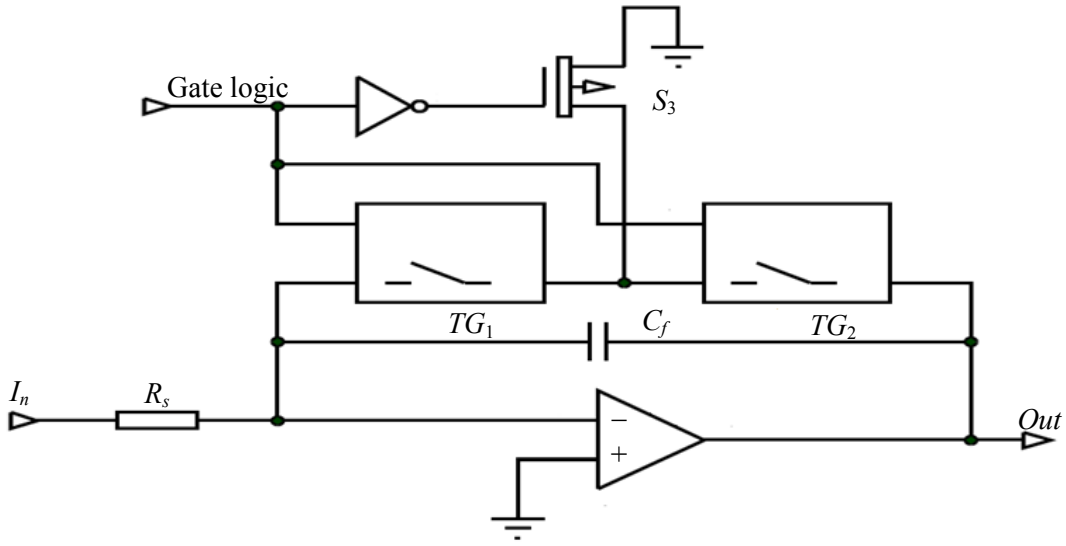


Fig. 9: A configuration switch as the reset switch

According to Equation (14), there is no leakage current when $I_{DS} = 0$, then the true option to obtain a zero switch leakage current is to set V_{DS} equal 0 V. To keep the V_{DS} of the MOS at zero, a configuration switch shown in Fig. 9 is used to replace the single reset switch from the gated integrator in Fig. 1. Two transmission gates switches, TG1, TG2, in series, compose the configuration switch with a grounded MOS switch, S3, attached to the node between the two transmission gates switches. When the two TG switches are off, the third switch, S3, is on. In this condition, V_{DS} of the transmission gate switch connected to the inverting input of the GI is kept at 0 V and no leakage current passes through this switch.

At the same time the used of transmission gate switches cancel the effect of the parasitic capacitances which produces the injection charges. When the MOS is on, some charges are present under the gate oxide resulting from the inverted channel. When the switch turns off, part of these charges will be injected into the capacitor C_{int}. For a NMOS the charge under the gate can be estimated by:

$$Q_{IN} = -C_{OX}WL\left(V_{GSN} - V_{THN}\right) \tag{15}$$

and for a PMOS the channel charge is:

$$Q_{IP} = -C_{OX}WL\left(V_{GSP} - V_{THP}\right) \tag{16}$$

It is noted that the injection charges are negative for NMOS and positive for PMOS. The problem is resolved by using a transmission gate switch to substitute the two MOS in series for T-switch configuration (Zhou *et al*., 2012). The transmission gate is composed of a NMOS and a PMOS connected in parallel controlled by complementary signals. Since it is known that the signs of the charges in an n-channel and in a p-channel in the Equation (15) and (16) are opposite, the charges injected from the n-channel and the p-channel will cancel out each other if their areas of gates are carefully designed shown in Fig. 9. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The control gates are biased in a complementary fashion so that both transistors are either on or off. As a switch a transmission gate, has turn-on non-zero channel resistance, which is better than the one of a single MOS switch.

Measurements and Discussions

In the laboratory, the measurements were made to characterize DC and AC performances of the circuit. The streaming signal generator XLV1 associated with voltage controlled current source was used to supply the input current signal to GI on the software program PSPICE. Specification of the New GI is shown in Table 2. Parameters were measured when the source current was in DC mode. All DC test results presented here and Fig. 10 shows the waveform of the GI made by configuration switch. The linearity of the GI is shown in Fig. 11.

Table 2: Specifications of the new GI

Parameter	Value
Full scale output	±5V
Voltage conversion gain	-1.0 V/V
Linearity error	<0.12%
Output voltage noise	<0.3mV (rms)
Output offset voltage	<0.5mV(rms)
Injected charge	<116pC
Temperature range	-40 to 125°C

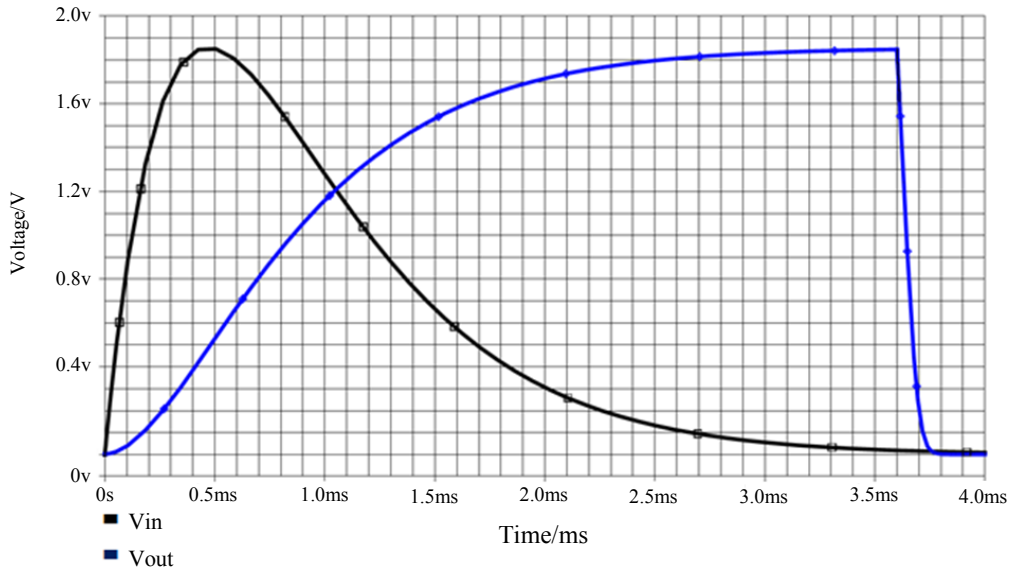


Fig. 10: Output waveform of the GI made by configuration switch of two transmission gates

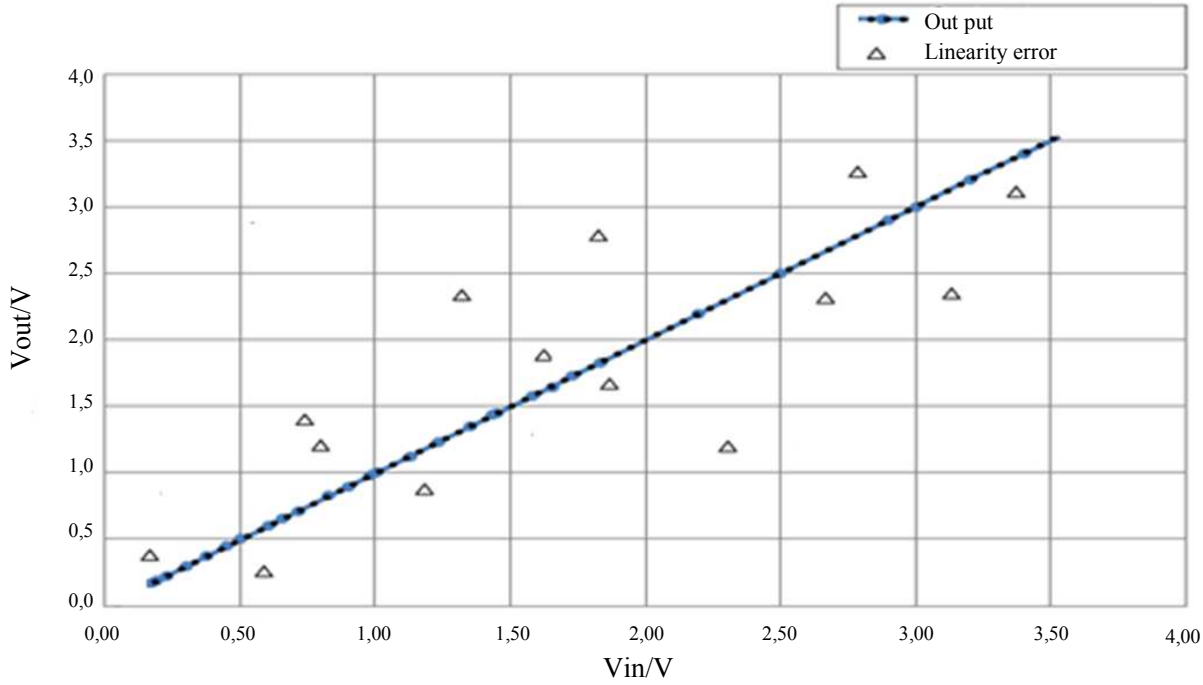


Fig. 11: Linearity of the GI

Conclusion

After developing the two new parts of the detector system, computer simulation was carried out by National instrument simulator to compare analytical results. The high degree of linearity was achieved by using a new configuration switch, which eliminated leakage current and reduced the charge injection from switches in the GI to *0.3mV*. Before the gated integrator, the new technique reduced the input current noise by using an inductor, which can be associated to a preventive capacitor. Results of the simulation show how intrinsic resistance of the inductor, determines the deepness of the noise reduction at the resonant frequency. The series *LC* circuit reduces the gate noise quantity to the input referred current noise at the resonant frequency, which establish at the 3 dB bandwidth of the TIA. The results of the simulation show that it had a high-resolution and stability. Then we can develop such a front-end circuit for read out weak signal.

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Author's Contributions

Ndalla Essengue Gloire: Performed some of the experiments through simulation software.

Wembe Tafo Evariste: Project leader, data interpretation and contribute to the writing of the paper.

Djamet Yimga Arnaud and Folla Kamdem Jérôme: Do part of d esign and simulations model. Also, contribute to the writing of the paper.

Essimbi Zobo Bernard: Project leader. Revise and improve the final drafts of the paper.

Ethics

The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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