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Design and Simulation of Novel Gated Integrator for the Heavy ion Beam Monitors System

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Abstract: In this study, the objective is to realize a Gated Integrator (GI) circuit for silicon strip, Si(Li), CdZnTe and CsI detectors etc. With the development of radioactive ion beam physics, heavy-charged particles like carbon ions have been applied to the treatment of deep-seated inoperable tumors in the therapy terminal of the Heavy ion Research Facility in Lanzhou (HIRFL) located at the Institute of Modern Physics (IMP), Chinese Academy of Sciences (CAS). A high resolution current measurement circuit was developed to monitor the beam current at 1pA range. The circuit consisted of a low current high sensitivity I/V converter and gated integrator in an energy spectroscopy. A low offset voltage precision amplifier and new guarding and shielding techniques were used in the I/V converter circuit which allowed to measure low current. This paper will show a MOS switch configuration which is used to prevent leakage current and novel technique to compensate a charge injection in the reset switch.

Keywords: Energy Spectroscopy, Noise, Gated Integrator, Charge Injection, Leakage Current Prevention

Introduction

The basic concept of gated integrator is to integrate signal as well as background when the image appears, to block or subtract the background when there is no image signal. Such procedures are executed numerous times for summation and averaging. Widely used imaging systems such as Si Charge Coupled Device (CCD), Complementary Metal-Oxide field effect transistor Active Pixel Sensor (CMOS APS), Schottky-Barrier Detector (SBD), InGaAs, InSb and HgCdTe FPAs are all based on the concept of current integration to accumulate signal in the purpose of improving the Signal-to-Noise Ratio (SNR), dynamic range and sensitivity. In Cooling Storage Ring (CSR) IMP Lanzhou, the main works are heavy ion beam accumulation, experiments related to cancer therapy, patients' treatment, mass measurement and prophase experiments on recombination (Kong *et al*., 2010; Zhang and Wu, 2011; Zhou *et al*., 2012). The main function of the electron cooler in the CSR is the accumulation of heavy ion beams. The efficiency of the accumulation was related with many parameters of storage ring and electron cooler, such as the work-point setting, closed-orbit, electron density and angle between the electron beam and the ion beam. Initially, the alignment of the electron beam was done to maximize the intensity of the accumulated ion beam. From November 2006, to 2012, around 106 patients have been irradiated in Lanzhou (HIRFL) at IMP, where carbon-ion beams with energies up to 100 MeV/μ can be supplied and a passive beam delivery system has been developed and commissioned (Li and Sihver, 2011). A number of therapeutic and clinical experiments (Kraft, 2000) on heavy-ion therapy were acquired at the IMP. To extend the heavy-ion therapy project to the treatment of a deep tumor, a horizontal beam line dedicated to this has been constructed in the CSR, which is a synchrotron connected to the HIRFL as an injector to be analyzed by detectors and is now in operation. A beam current monitoring circuit was necessary and urgent to calibrate these detectors. Beams applied to treatment are less than 1 pA. These low beams current are modulated because of operating modes of a synchrotron and also suffer from poor accuracy (Kong *et al*., 2010; Auzelyte *et al*., 2006).

This paper presents a description of a low current measurement circuit for the beam current monitor system. In detail the paper will describe the structure of GI based on leakage current, charge injection, noise

analysis and introduction of a switch technique with high sensitivity when comes the measurement of low current. It also shows that the noise analysis during a transient voltage excursion appeared at the gate can sense the readout system.

GI in the Beam Monitors System

Figure 1 shows the block diagram of the heavy ion beam current monitor system. The low current measurement circuit consists of I/V Converter and a GI (Sun *et al*., 2003). The current signal from the Faraday cup (FC), which was pulsed for 0.5ms a period of 4ms, was converted into a voltage signal through a I/V Converter, the output of which was integrated by the GI in order to measure the charge of the beam (Kong *et al*., 2010; Redondo *et al*., 2007; Hori and Hanke, 2008). Outputs of I/V Converter and GI were acquired by a data acquisition system based on PXI.

Compared to traditional current gated integrators (Kong *et al*., 2010; Riboldi *et al*., 2010), which integrated the current from the FC by a GI directly, the new circuit prevented many disturbances like leakage current of the feedback capacitor and charge injection of switches.

The Design of the New GI

A gated integrator is designed to recover fast, repetitive, analog signals with time scales ranging from 10^{-11} to 10^{-4} seconds. In a typical application, a time window within a certain width is "gated" after a set delay from an internal or external trigger. A gated integrator amplifies and integrates the signal that is present during the time the gate is open, excluding noise and interference that may be present at other times. Since any signal present while the gate is open will add linearly, while noise will add in a "random walk" fashion as the square root of the number of shots, prevent leakage and charge injection compensation will improve the SNR. The gated integrator is actually a Capacitive Transimpedance Amplifier (CTIA) except the gated switch, so it also performs as a low pass filter. To get the total charge of the beam, the output of the I/V converter was fed into the GI, the schematic indicated by the dotted line in Fig. 1. The input signal voltage V_i is converted into current via the resistor R_S and integrated by the feedback capacitor C_f. The output voltage V_{out} is given by:

$$V_{out} = \frac{1}{C_f R_S}\int_0^T V_i(t)dt + V_0 \quad (1)$$

Since the input voltage V_i, is proportional to the current from the *FC*, the GI output V_{out}, represents the total charge of the beam for a given duration *T*. The leakage current elimination techniques and charge injection compensation were implemented in the GI section. The GI circuitry is composed of switches, operational amplifier and capacitors. The non-ideal switch and amplifier will introduce additional noise and fixed pattern (Levinzon, 2005; Wembe *et al*., 2014). The goal of the design is trying to understand the issues and take appropriate strategies to limit them such that the performance of the circuitry is not overshadowed.

Characteristics of MOS Switch

The main features of a MOS switch are switch speed, charge injection and clock feedthrough. The rise and fall times of a submicron gate switch is usually less than 0.1 ns. This can impose a problem only in readout circuit of extremely high speed Focal Plane Array (FPAs). The charge injection and clock feedthrough, however, are the main sources of noises in a MOS switch.

A switch is used to pass voltage or current. An ideal switch has the characteristics of zero resistance when it is ON, infinite resistance when it is OFF and no delay when it is turned ON or OFF. A real MOSFET switch however, has turn-ON non-zero channel resistance, turn-OFF leakage current, threshold voltage and parasitic capacitances.

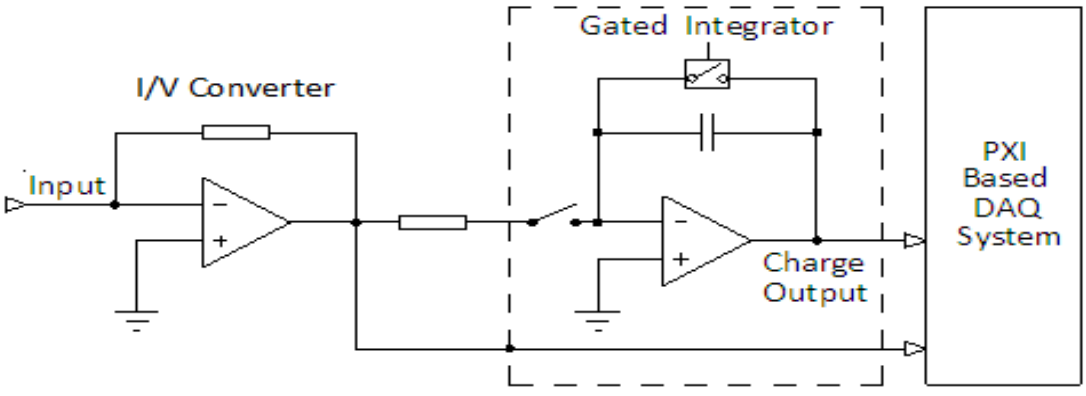

Fig. 1. Block diagram of the heavy-ion beam monitor system

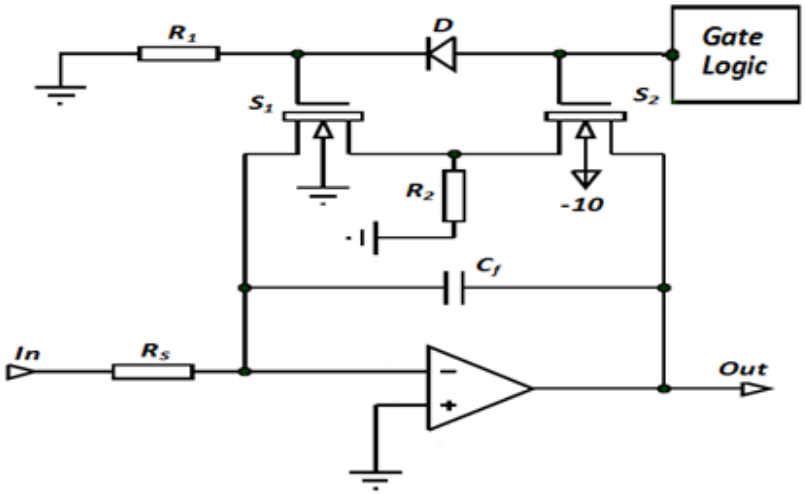

Fig. 2. A switch configuration as the reset switch

MOS Switch Configuration to Prevent Leakage Current

While the Gated Integrator (GI) is in "integration" or "hold" state, the effect reset switch has to be kept OFF. However the effect of leakage current in the GI reset switch will cause errors to the output in the long duration of these states. The problem can be resolved by using the CMOS switch configuration to replace single reset switch shown in Fig. 2.

Although both n-channel MOSFETs integrator, are switched together, S_1 is switched with gate voltages of zero and +5 volts so that gate leakage (as well as drain-source leakage) is entirely eliminated during the OFF state (zero gate voltage). In the ON state the capacitor is discharged as before, but with twice R_{ON}. In the OFF state, one has in S_2 small leakage which passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because S_1's source, drain and substrate are all at the same voltage. If the source and body are at the same potential, the drain-source current of a MOS transistor in the deep sub-threshold region of operation is given by:

$$I_D = KI_{DO} \cdot \exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (2)$$

$$I_{D0} = \mu_n C_{OX}(\eta - 1)V_T^2$$

where, I_D is the drain to source current of the transistor MOS, K is the aspect ratio of the transistor, I_{DO} is the saturation current, V_{GS} is the gate to source voltage, V_{th} is the threshold voltage of a MOSFET, V_T is the thermal voltage, V_{DS} is the drain to source voltage, μ_n is the carrier mobility, C_{OX} is the gate oxide capacitance and η is the sub-threshold slope factor (Redondo *et al*., 2007; Riboldi *et al*., 2010; Ueno *et al*., 2010 and Taur and Ning, 2002). Equation 2 shows, even for V_{GS} = 0, the only way to establish a zero switch leakage current is to set V_{DS} to 0 *V*. To maintain the V_{DS} of the MOSFET switch at virtual ground, a MOS switch configuration shown in Fig. 2, is used to replace the single reset switch from the gate integrator in Fig. 1. The MOS switch configuration is composed of two MOSFETs switches, S_1, S_2, in series and a grounded resistor, R_2, attached to the node between the two switches. When the two MOS switches in parallel with the storage capacitor are OFF, in S_2, a small leakage passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because S_1's source, drain and substrate are all at the same voltage. Thus, in this configuration, V_{DS} of the switch connected to the inverting input of the integrator is maintained at *0 V* and zero or very little leakage current flows through this switch.

Charge Injection Compensation

MOS switches were chosen as switches in the GI. When a transient voltage excursion appeared at the gate, there would be an injection of electric charge into analog path via the gate-to-drain and the gate-to-source capacitances, which would cause errors to the GI output. The circuitry for electrical injection indicated by the dotted line in Fig. 3 was used to compensate error cause by this charge injection. When the state of switches is changed, certain quantity of charge will be injected into the inverting input via the capacitor C_C by the compensation network. This is opposite to the charge injected by switches. Since it is known that the amount of charge injected is equal to the product of the voltage excursion amplitude on the component and its

capacitance, generating a product equal magnitude but opposite polarity can be used to compensate for this effect. After analysis and experimental trials, C_C was chosen to be 10 *pF* from the Equation 3. Thus by changing the amplitude of the voltage excursion on C_C, the error of the output voltage caused by charge injection was reduced to less than 0.7 *mV*:

$$Q^f = C_C V_S^f + C_{GS}\left(V_S^f - V_G\right) \text{ when}$$
$$V_S^f = \frac{R_1' V_{EE} + R_2' V_G}{R_1' + R_2'} \quad (3)$$

where, Q^f which is the final charges stored at node V_S, V^f_S is the final stable voltage at node V_S, V_G is the gate logic voltage, V_{EE} is biasing voltage for the injection compensation circuit, C_{GS} is the gate-to-source capacitance, R'_1 and R'_2 are resistances of the potentiometer and C_C the capacitor of the compensation network.

Measurements and Discussions

The measurements were developed in the laboratory in order to characterize DC and AC performances and efficiency of the circuit. The streaming signal generator XLV1 associated with voltage controlled current source was selected to supply input current signal to GI on the software program PSPICE. Specification of the New GI is shown in Table 1. Parameters were measured when the source current was in DC mode. All DC test results presented here, including linearity shown in Fig. 4.

In order to recover the signal from the measurement system, simulation from Fig. 5, shows how single switch does not prevent leakage current. Then it will be difficult to recover the total signal. To prevent this effect, the single reset switch is replaced by the MOS switch configuration shown in Fig. 2, then the leakage current will disappear see Fig. 6, but we still remark an error appearance when the switch turns ON. This error is from the charge injection. During the rising edge of the clock signal of the gate, the gate starts at 0 volts and increases toward high voltage. In the transition from 0 to $V_{in} + V_{th}$, the switch is OFF. Consequently, this part of the clock waveform can couple to C_{int} via C_{GS}. As a result, a portion of the clock signal appears across C_{int} as indicated on the Fig. 6, during the transition at 3.8 ms. The circuitry indicated by the dotted line in Fig. 3, was used to compensate the charge injection see the simulation result in Fig. 7.

In contrast to charge injection when the switch is turned from ON to OFF, there is charge absorption when the switch is turned from OFF to ON for successive readout signal, which will cause an error shown in Fig. 8. for second and third readout during a low current measurement. We solve the problem by using a slow change clock to turn OFF the switch, Fig. 9. This results because the charges in the channel will be mostly injected into the substrate.

Table 1. Specifications of the new GI

Parameter	Value
Full scale output	±5 V
Voltage conversion gain	-1.0 V/V
Linearity error	<0.06%
Output voltage noise	<0.7 mV (rms)
Output offset voltage	<0.5 mV(rms)
Injected charge	<116 pC
Temperature range	-40°C to 125°C

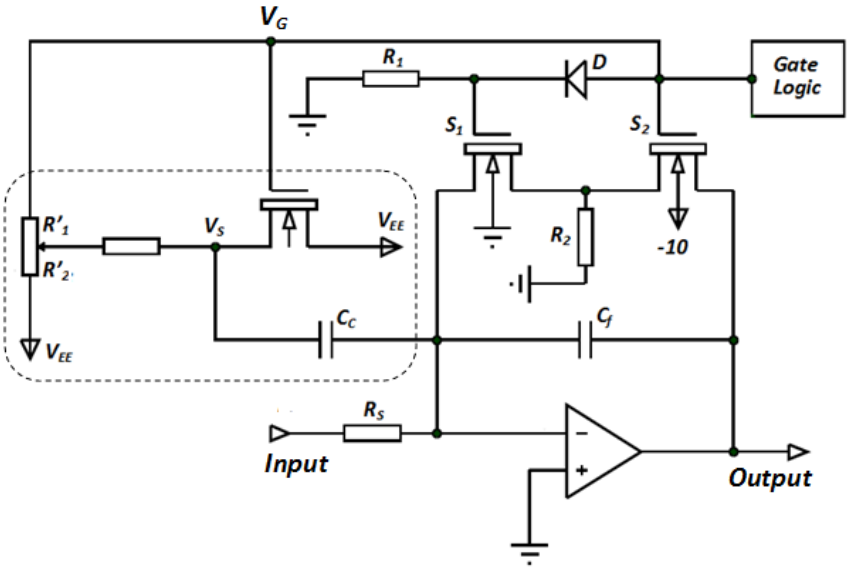

Fig. 3. Schematics of the GI with a network for charge injection compensation

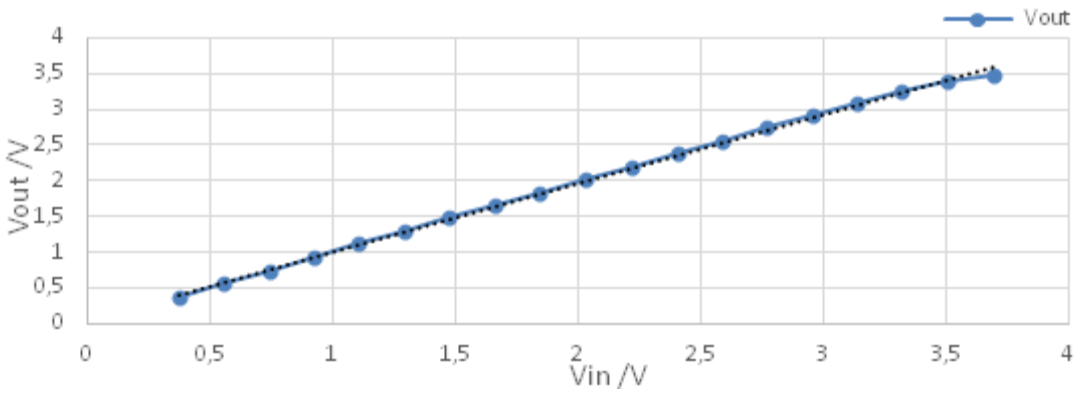

Fig. 4. Linearity of the GI

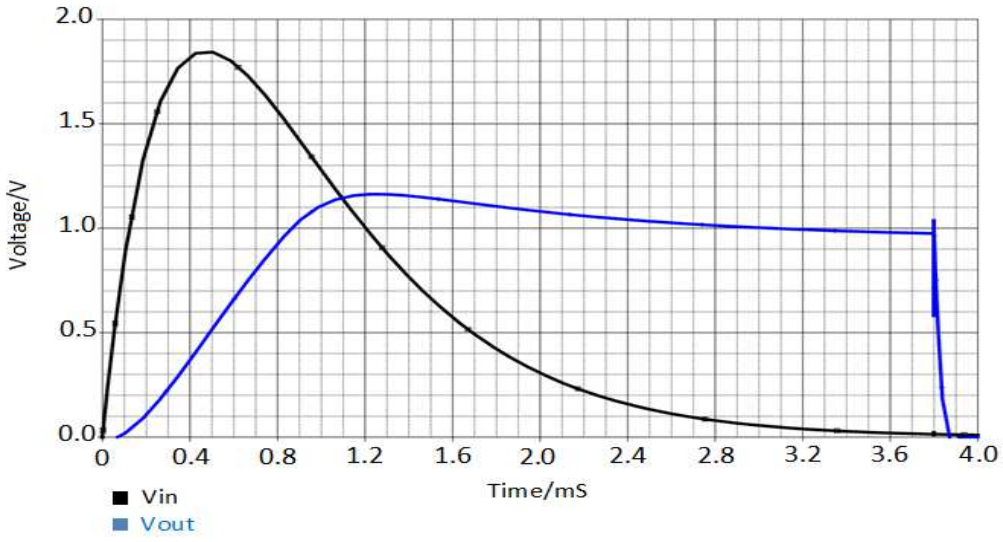

Fig. 5. Output waveform of the GI from I/V Converter output using a single reset switch

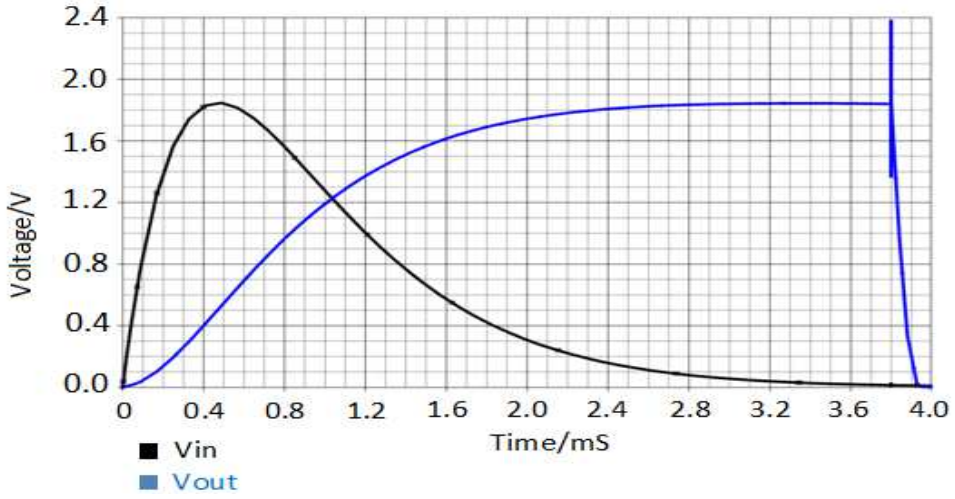

Fig. 6. Output waveform of the GI from I/V Converter output using switch configuration made by two NMOSFETs

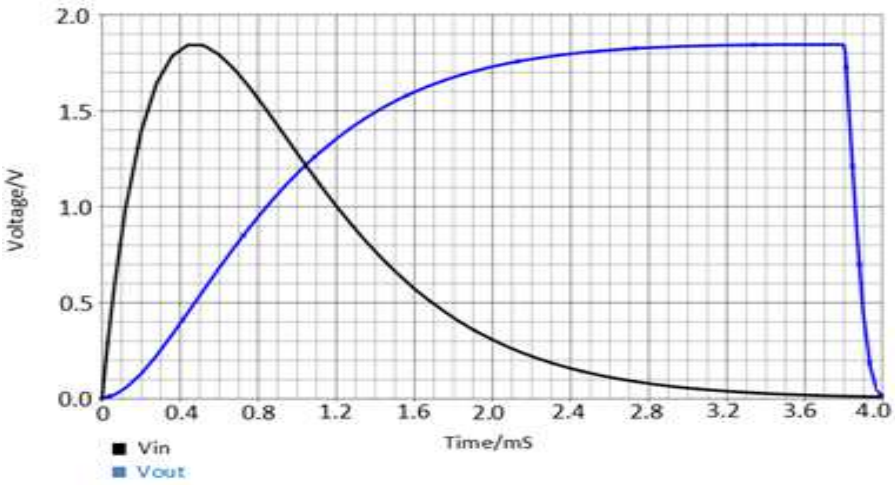

Fig. 7. Output waveform of the GI from I/V Converter output using switch configuration made by two transmissions gated to prevent charge injection

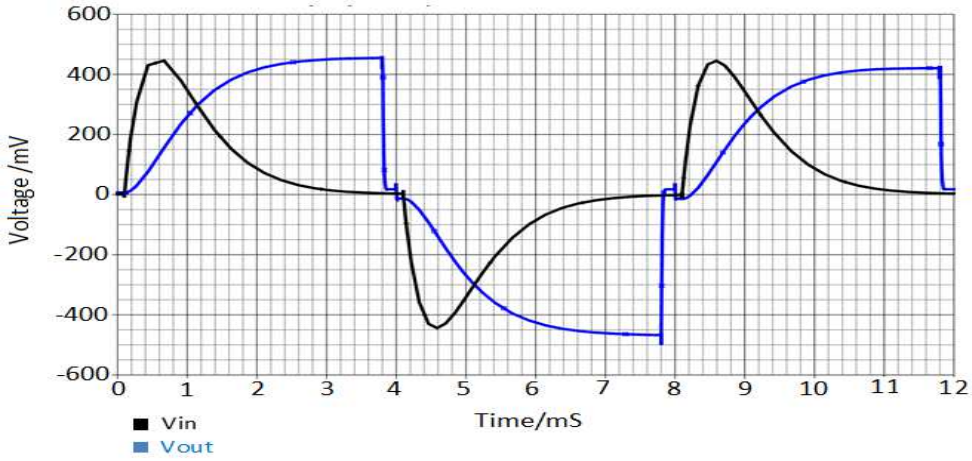

Fig. 8. Fast change clock to turn OFF the switch

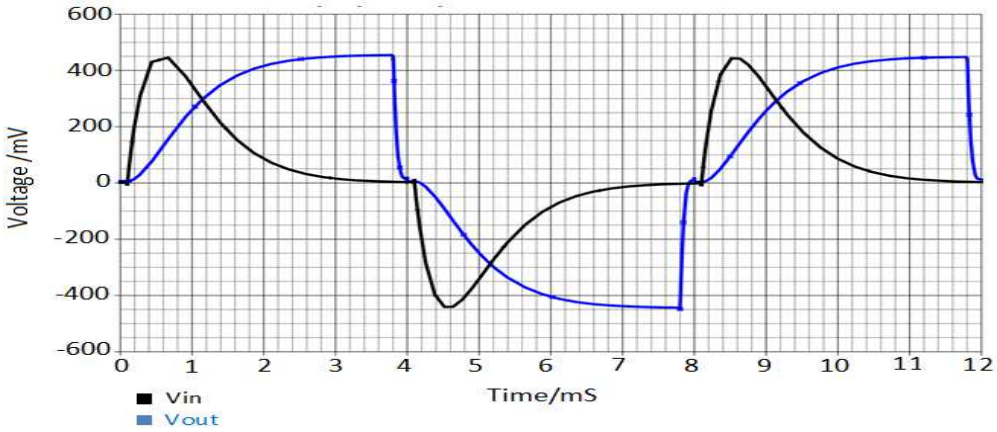

Fig. 9. Slow change clock to turn OFF the switch

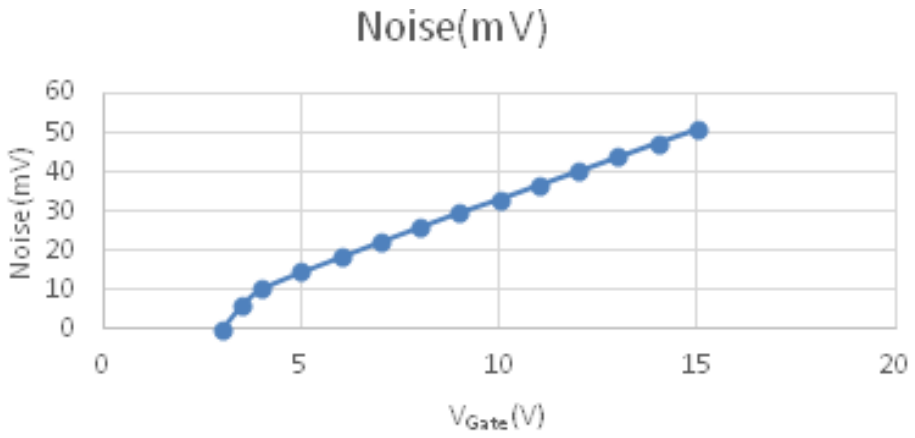

Fig. 10. Noise effect for the integrator versus clock voltage gate

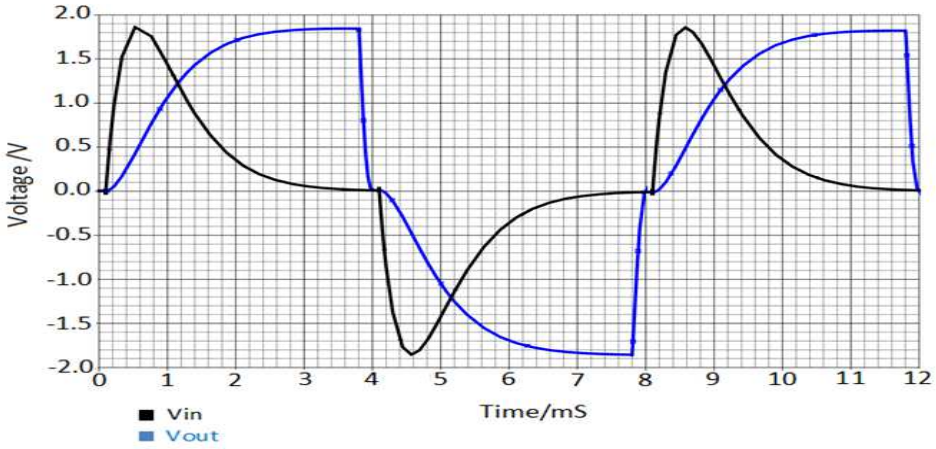

Fig. 11. Fast and slow change clock to turn OFF the switch with substantial value measurement

The injected charge induces fixed pattern noise, which will limit the minimum detectable signal. To choose a proper voltage for the clock signal of the gate to reduce pattern noise even though we use a rapid change clock, the analysis of noise effect is developed. The simulation results show that the number of these charges varies with the voltage of the gate. They are shown in the Fig. 10. One can just find a difference among the Fig. 8, 9 and 11. The simulation results show how noise effect appears when we are measuring low values and disappear with slow change clock. This noise effect is also negligible or disappears when the measurement is substantial.

Conclusion

After designing the new circuit, computer simulation was carried out by PSPICE simulator. The high degree of linearity was achieved by using a novel switch configuration, a new compensation approach which reduced the charge injection from switches in the GI to 0.7 mV. The results of the simulation show how noise effect appears when we are measuring low values and disappear with slow change clock. This noise effect is also negligible or disappears when the measurement is substantial. The results of the simulation of a low and medium current measurement circuit show that it had a high resolution and stability. Because of the circuit design techniques used for high event rate capability insured that the circuit would perform well in high-resolution energy systems for the heavy ion beam monitors.

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Author's Contributions

Wembe Tafo Evariste: Project leader, data interpretation and contribute to the writing of the paper.

Djamet Yimga Arnaud: Design and simulations model. Also, contribute to the writing of the paper.

Essimbi Zobo Bernard: Project leader. Revise and improve the final drafts of the paper.

Ethics

The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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