

Application Specific Integrated Circuits Design and Implementation of Rademacher and Walsh Functions

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ABSTRACT

The orthogonal functions, specially the Rademacher and Walsh functions are being increasingly used in Digital Signal Processing (DSP). Today's DSP applications require fast processing time in order to meet the challenges of the real time systems. State-of-the-art implementation technologies are therefore being used. This study describes the design and implementation of Rademacher and Walsh functions targeted to the state-of-the-art Cell Based Integrated Circuits (CBIC) technology. High level design techniques are used with the help of advanced EDA tools from SYNOPSIS International. Optimized VHDL models have been developed and used for design entry. The design is thoroughly verified using advanced verifications tools. The design is implemented and processing has been done with 90 nm CMOS Technology from TSMC foundry. It is observed that the results obtained, are far better than the FPGA implementation reported earlier in the literature.

Keywords: ASIC, CBIC, Rademacher Functions, Walsh Functions

1. INTRODUCTION

Digital Signal Processing is well known for processing of digital signals and it requires high speed and fast processing time to meet today's real world applications. With developing technology, more complex algorithms are evolving. Therefore to realize these algorithms for real world applications hardware implementation is necessary. Field Programmable Gate Arrays (FPGAs) are good choice for hardware realization but with limitations in design optimization. Furthermore, FPGA implementation is good for prototyping where, the aim is to predict the behavior of design in real world applications, there are many DSP systems reported in literature few of them are (Palaniappan and Zulkifli, 2007; Benhamid and Othman, 2009; Rais *et al.*, 2010; Rais, 2010; Teymourzadeh *et al.*, 2010). Application Specific Integrated Circuits (ASIC) is the most feasible technology to realize DSP algorithms

and any other complex algorithm, without much limitations in optimizing the design. Furthermore, as the technology is emerging, fabrication of increasingly larger number gates is becoming possible in an ASIC that makes it highly appropriate for large and complex designs. Cell Based Integrated Circuits (CBIC) is a type of ASICs. CBIC uses predesigned logic cells known as standard cells. The standard cells areas in a CBIC are built of rows. The standard cell area can also be used for Macro cells. All the mask layers of CBIC are customized and are unique to a particular design. The most prominent advantage of CBIC is to use the predesigned, pre-characterized and pretested standard cells. ASIC manufacturer provides detail data of standard cell, with complete description of metal layers, routing protocols and power/ground recommended flow.

In the present work, Rademacher functions and Walsh functions are realized by using state of the art

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ASIC technology. High level designing techniques are adopted and design is modeled in VHDL language (Benmohammed and Merniz, 2005; Abbasi *et al.*, 2010). Simulation and verification is achieved by using advanced EDA tools from Synopsys. Synopsys tools are widely used for chip and device designing (Hashim and Rasmi, 2006; Maiti and Maiti, 2010). Physical Layout designing is also done in Synopsys innovative Backend tools. Top down design methodology is adopted.

2. MATERIALS AND METHODS

2.1. Rademacher Functions

The function $f_n(x)$ is defined on the closed interval $[0,1]$ by the Equation (1) (Wolfram, 2002):

$$f_n(x) = \text{Sgn}[\sin(2^n \pi x)], n = 0,1,2,3,\dots \quad (1)$$

Where:

$$f_0(x) = 1$$

Sgn = The Signum Function Equation (2)

$$\text{Sgn}(y) = \begin{cases} +1, y \geq 0 \\ -1, y < 0 \end{cases} \quad (2)$$

By Periodicity property (Wolfram, 2002) of Rademacher Function, it can be extended over the whole non negative real line Equation (3):

$$f_0(x+1) = f_0(x) \quad (3)$$

Rademacher functions form an incomplete set of orthogonal functions (Rath and Meher, 2007), from which subset of Walsh Functions can be formed Equation (4):

$$f_n(x) = \lim_{\epsilon \rightarrow 0} f_n(x + \epsilon) \quad (4)$$

Figure 1 shows the first 5 Rademacher functions.

2.2. Walsh Functions

Analysis of a signal is a very important task in science and engineering problems. From decades, Fourier theory has been a very important tool in analyzing signals, particularly for the analysis of analog signals where sine-cosine functions are used. However, with the advent of digital computers and their use in different fields, theory of Discrete Fourier Analysis has to be further developed (Palaniappan and Zulkifli,

2007). For Discrete Signal Analysis, there are many other theories to analyze them and sometimes they gives better result than discrete fourier analysis. One of the theories is based on a set of Walsh Functions (Wolfram, 2002; Maqusi, 1981).

Walsh functions consist of sequence of square pulses between -1 and +1, the transitions only occurs at fixed intervals and initial state is always +1 (Thompson *et al.*, 2008). Walsh functions were first used by Frank Fowle, an electrical engineer; to find the transpositions of wires that minimized the crosstalk and later it is introduced in mathematics by Walsh (Wolfram, 2002).

Walsh used an unattractive notation for set of functions, which is inconvenient for analytical computation. However, its definition is largely adopted by engineers and scientists for computational purposes.

Various researchers developed interest in Walsh theory and generated several other types of formulae (Wolfram, 2002), in particular, to generate Walsh functions for digital computation and to develop more attractive notation for analytical and mathematical solutions. Scientists found that Walsh functions can also be evaluated from Rademacher functions (Maqusi, 1981; Wolfram, 2002; Karpovsky *et al.*, 2008) and Rademacher functions can easily be generated by using a counter (Ateeq *et al.*, 2002; Qasim and Abbasi, 2006).

Harmuth's development of Walsh Functions are defined by the following recursive formula (Wolfram, 2002) Equation (5):

$$\text{wal}_{2^{j+p}}(x) = -1^{\frac{j+p}{2}} \left\{ \begin{array}{l} \text{wal}_j \left\{ 2 \left(x + \frac{1}{4} \right) \right\} + (-1)^{j+p} \\ \text{wal}_j \left\{ 2 \left(x - \frac{1}{4} \right) \right\} \end{array} \right\} \quad (5)$$

Where:

$$p \in \{0,1\}$$

$$j = 0,1,2,\dots \text{ Equation (6):}$$

$$\text{wal}_0(x) = \begin{cases} 1, -\frac{1}{2} \leq x < \frac{1}{2} \\ 0, \text{otherwise} \end{cases} \quad (6)$$

This definition formulates the set of Walsh functions in unit time interval $[-1/2, 1/2)$. Parameter $\text{wal}_m(x)$ indicates the average number of zero crossings in a unit interval. This parameter is named as "sequency" and it also indicates an ordering of Walsh function in a

sequence. Where $(m = 0, 1, 2, \dots)$ and it can be defined as (Wolfram, 2002):

Sequency = average number of zero Equation (7):

sequency = average number of zero crossings in a unit interval (7)

The even Walsh functions $Cal(m)$ and the odd Walsh functions $Sal(m)$ as (Wolfram, 2002) Equation (8 and 9):

$$Cal_n(m) = Cal(n, m) = W_n(2m + 1) \tag{8}$$

$$Sal_n(m) = Sal(n, m) = W_n(2m) \tag{9}$$

These terms are derived from the longer names “Cosine-Walsh” and “Sine-Walsh”.

Let the set of Walsh functions defined on $[0, 1)$. Then Equation (10 and 11):

$$\psi_0(x) = 1, 0 \leq x < 1 \tag{10}$$

And

$$\Psi_n(x) = \prod_{i=0}^N [\phi_{i+1}(x)]^{n_i}, n_i \in \{0, 1\} \tag{11}$$

where the integer n is assumed to be dyadic (binary) representation Equation (12):

$$n = \prod_{i=0}^N 2^i n_i \tag{12}$$

Such representation is good for considering basic characteristics of Walsh functions. **Figure 2** shows the first eight Walsh functions defined on the unit interval $[0, 1)$.

Incidentally, the Walsh functions $\Psi_n(x)$ may be defined on the unit interval $[-1/2, 1/2)$ by a simple shift of their graphs. Naturally this follows easily from their periodicity characteristics. Under such a definition, the functions $\Psi_n(x)$ may be related to the sequency-ordered set $wal_n(x)$ via the following relation Equation (13):

$$wal_n(x) = \begin{cases} \Psi_{\frac{n}{2} \oplus n}(x), & n = 0, 2, 4, \dots \\ \Psi_{\frac{n-1}{2} \oplus n}(x), & n = 1, 3, 5, \dots \end{cases} \tag{13}$$

An interesting result connects the dyadic representation of a real number x and associated Walsh function $\Psi_n(x)$. Thus let x be a nonnegative real number.

This number may then be represented by a dyadic expansion as Equation (14):

$$x = \sum_{i=-\infty}^N 2^i x_i = [x] + \sum_{i=1}^{\infty} 2^{-i} x_i, x_i \in \{0, 1\} \tag{14}$$

where, (x) denote the largest integer in the real number x .

The expansion coefficients x_i associated with a real number x are related to Rademacher functions by Equation (15 and 16):

$$x_{i+1} = \frac{1}{2}[1 - \phi_i(x)], i = 0, 1, 2, \dots \tag{15}$$

Hence:

$$x_{i+1} = \frac{1}{2}[1 - \psi_{2^i}(x)], i = 0, 1, 2, \dots \tag{16}$$

Since Equation (17):

$$\psi_{2^i}(x) = \phi_i(x), i = 0, 1, 2, \dots \tag{17}$$

2.3. CBIC Design

2.3.1. Design of Rademacher Functions

Rademacher functions are generated by considering Equation (1), where $f_0(x) = 1$.

For $n = 1$, splits the $f_0(x) = 1$ to half between interval $(0, 1)$ and put first half of a function as “+1” and second half as “0”.

For $n = 2$, $f_1(x)$ is further divided into four segments in interval $(0, 1/2)$ and $(1/2, 1)$. First half of both intervals considered as “+1” and second half of both intervals considered as “0”.

Similarly each function can be divided into this manner to get the values of next function. It has been observed that simple binary counter can also depict this signal generation at various output stages. So we omit the complex VHDL coding for the Equation (1) and generate a simple 5 bit binary counter for the generation of Rademacher functions:

```
Snippet of VHDL coding.
RADFUNC: process (clk, reset)
    Begin
        if reset = '1' then
            temp <= "00000";
        elsif (clk'event and clk = '1') then
            temp <= temp + 1;
        end if;
    end process RADFUNC;
```

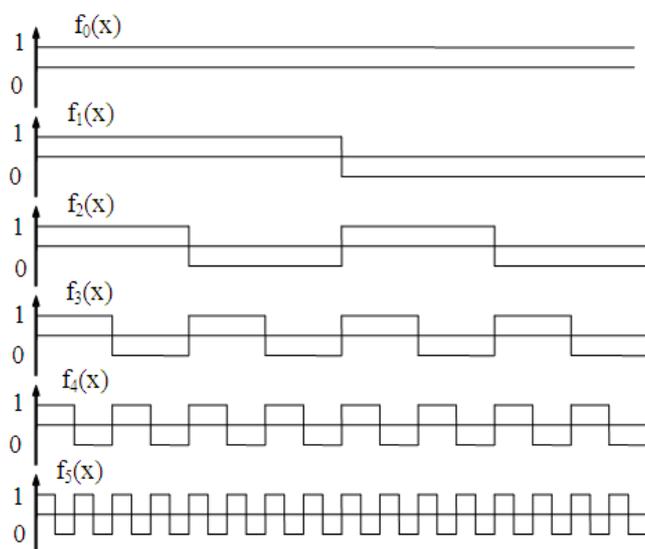


Fig. 1. First five rademacher functions

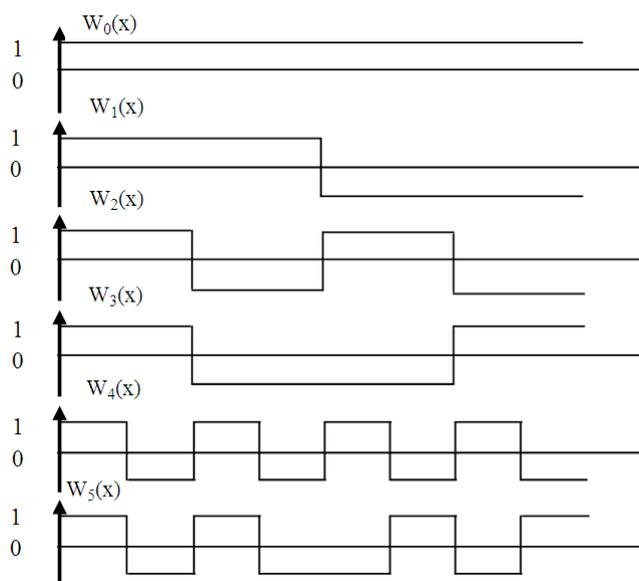


Fig. 2. The first six Walsh functions

2.3.2. Design of Walsh Functions

Walsh functions are generated by using Equation (10 and 11). Walsh functions of different orders are calculated with the product of appropriate Rademacher functions, based on the gray code conversion of the Walsh function index sequence. We convert the ± 1 amplitude of the Walsh function into binary representation by making $+1 \rightarrow '0'$ logic and $-1 \rightarrow '1'$

logic. Multiplication of Rademacher functions is now equivalent to Exclusive-OR operation. Snippet of the VHDL code is as follows:

```

WAL(1) <= not TEMP(4);
WAL(2) <= not TEMP(3);
WAL(3) <= not (TEMP(4) xor TEMP(3));
WAL(4) <= not TEMP(2);
WAL(5) <= not (TEMP(4) xor TEMP(2));
    
```

WAL(6) <= not (TEMP(3) xor TEMP(2));
 WAL(7) <= not (TEMP(4) xor TEMP(3) xor TEMP(2));
 WAL(8) <= not TEMP(1);
 WAL(9) <= not (TEMP(4) xor TEMP(1));
 WAL(10) <=not (TEMP(3) xor TEMP(1));
 WAL(11) <=not (TEMP(4) xor TEMP(3) xor TEMP(1));
 WAL(12) <=not (TEMP(2) xor TEMP(1));
 WAL(13) <=not (TEMP(4) xor TEMP(2) xor TEMP(1));
 WAL(14) <=not (TEMP(3) xor TEMP(2) xor TEMP(1));
 WAL(15) <=not (TEMP(4) xor TEMP(3) xor TEMP(2)
 xor TEMP(1));
 WAL(16) <=not TEMP(0);
 WAL(17) <=not (TEMP(4) xor TEMP(0));
 WAL(18) <=not (TEMP(3) xor TEMP(0));
 WAL(19) <=not (TEMP(4) xor TEMP(3) xor TEMP(0));
 WAL(20) <=not (TEMP(2) xor TEMP(0));
 WAL(21) <=not (TEMP(4) xor TEMP(2) xor TEMP(0));
 WAL(22) <=not (TEMP(3) xor TEMP(2) xor TEMP(0));
 WAL(23) <=not (TEMP(4) xor TEMP(3) xor TEMP(2)
 xor TEMP(0));
 WAL(24) <=not (TEMP(1) xor TEMP(0));
 WAL(25) <=not (TEMP(4) xor TEMP(1) xor TEMP(0));
 WAL(26) <=not (TEMP(3) xor TEMP(1) xor TEMP(0));
 WAL(27) <=not (TEMP(4) xor TEMP(3) xor TEMP(1)
 xor TEMP(0));
 WAL(28) <=not (TEMP(2) xor TEMP(1) xor TEMP(0));
 WAL(29) <=not (TEMP(4) xor TEMP(2) xor TEMP(1)
 xor TEMP(0));
 WAL(30) <=not (TEMP(3) xor TEMP(2) xor TEMP(1)
 xor TEMP(0));
 WAL(31) <=not (TEMP(4) xor TEMP(3) xor TEMP(2)
 xor TEMP(1) xor TEMP(0));

3. RESULTS

Chip designing is a highly sophisticated work that requires many steps to achieve the desired design. Chip designing also requires highly sophisticated and specialized EDA tools, which play very important role in de-signing a chip. This is because at each step, the designer needs to optimize the design to the best achievable limit and this can only be done with the help of highly specialized tools (Palaniappan and Zulkifli, 2007). Synopsys is one of the leading company in the manufacturing of EDA tools and this design is implemented by using complete CBIC design suite of soft-wares from Synopsys.

3.1. Supporting Tools

Synopsys Tools used for designing are as follows.

3.1.1. For Front End Design

- Functional Verification is done from VCS
- Design Synthesis is done from Design Compiler (DC)
- Formal verification of Synthesized Database by Formality
- Prelayout Static Timing Analysis by Primitime

3.1.2. For Back End Design

- Floor planning, Placement, Clock tree synthesis and Routing done by IC Compiler
- DRC and LVS checks are done by Hercules
- Layout Parasitic extraction achieved from StarRC
- Post layout Static timing analysis is also done by Primitime
- Formal Verification of hardcore design verified from Formality

3.2. Simulation of Rademacher Functions

Simulation results of Rademacher functions are shown in **Fig. 3**.

These results are generated after backend design. Star RC is used to extract the parasitics of a design and generate Standard Parasitic Extraction File (SPEF) which is then fed to Prime Time, for Post Layout Static Timing Analysis.

3.3. Simulation of Walsh Functions

Walsh functions simulation results are shown in **Fig. 4**.

Design is verified behaviorally, after performing Layout designing. Delays are measured at different instances of the clock as shown in **Fig. 5**. Maximum delay is found to be 3.1 ns.

4. DISCUSSION

The design is targeted to TSMC 90 nm CMOS Low Power (LP) High Threshold Voltage (HVT) technology. In 90nm technology, 9 metal layers fabrication process is adopted, in which odd numbered metal layer can only be used for horizontal connections and even numbered can only be used for vertical connections. Metal layer 1 is used for standard cells placement, Metal layer 2 used for vertical clock and signal routing, Metal layer 3 is used for horizontal clock and signal routing, Metal layer 4 to Metal layer 9 is mainly used for power and ground straps. However, some of the signal routing also occurs from Metal layer 4 to Metal layer 7 to avoid DRC errors.

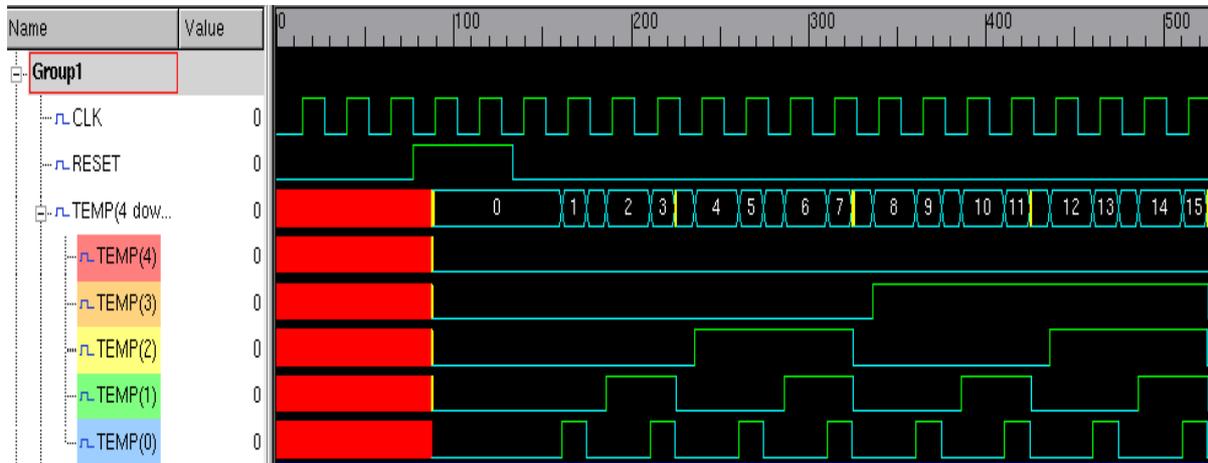


Fig. 3. Simulation results of rademacher functions

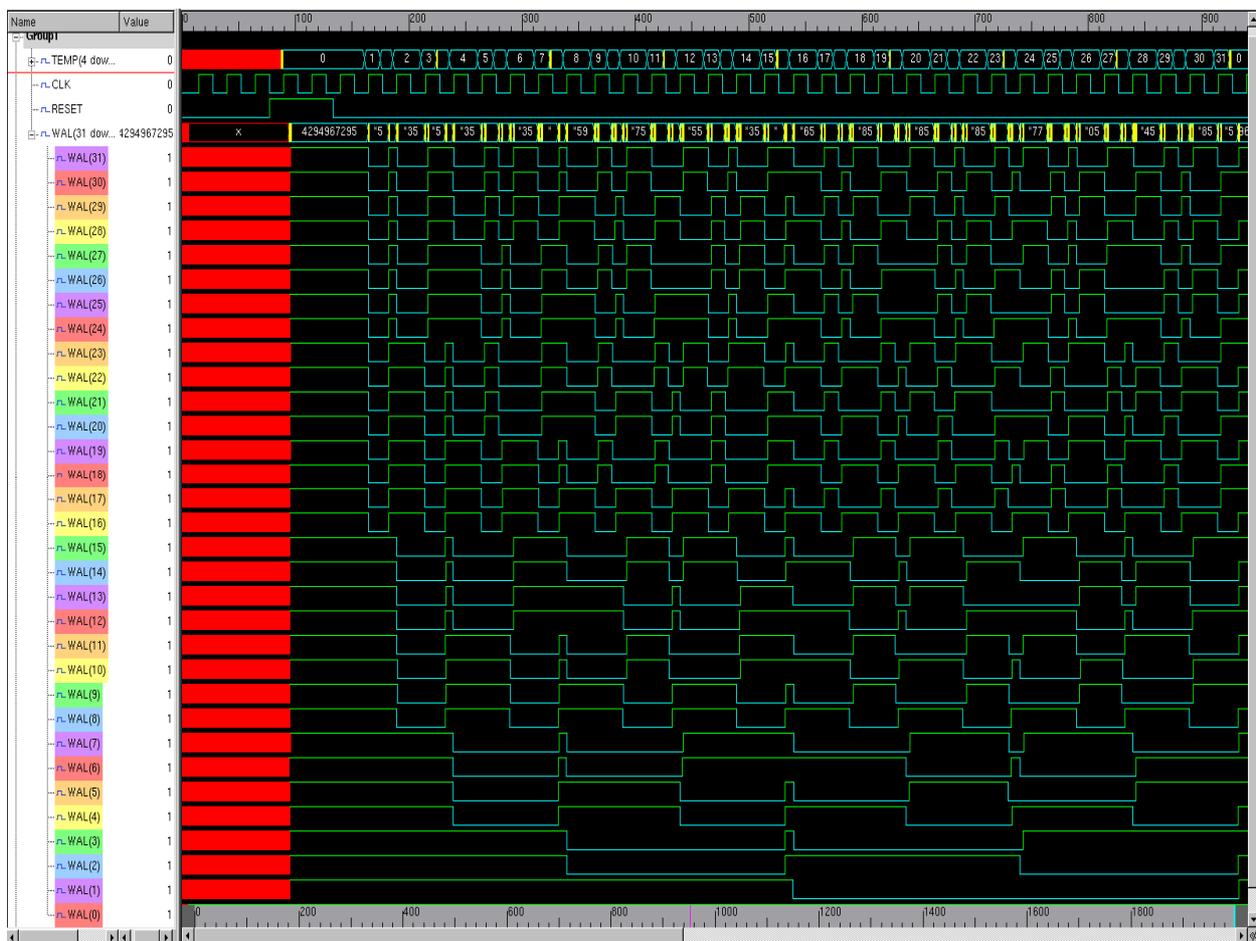


Fig. 4. Post layout simulation results of walsch functions



Fig. 5. Timing delays of Walsh functions

Table 1. Power analysis

Dynamic power	Watts(mW)
Dynamic power	
Cell internal power	0.0269193
Net switching power	5.60800
Total dynamic power	5.634900
Cell leakage power	
Total cell leakage power	0.171263×10^{-3}

Table 2. Detailed power analysis

Power group	Internal power (mW)	Switching power (mW)	Leakage power (mW)	Total power (mW)
Register	5.7214×10^{-3}	0.2844	8.1327	0.2901
Combinational	2.1198×10^{-2}	5.0392	163.1291	5.0606
Total	2.6919×10^{-2}	5.3236	171.2618	5.3507

Metal layer 8 and Metal layer 9 are specifically for power mesh, which is connected to the power ring, in the surrounding of core area. Power Mesh is also connected to the Metal layer 1 through Vias. Summary of Power analysis is shown in **Table 1 and 2**. Area and number of different cells used in this implementation are shown in **Table 3**. Total area for this

implementation is 94 mm^2 out of which 74 mm^2 is dedicated to core area where all the routing and standard cells are placed. Rest of the 20 mm^2 is used for I/O Ports cells and power ring. Chip utilization ratios are depicted in **Table 4**. **Table 5** contains the Chip and core information and **Table 6** shows the information of each metal layer.

Table 3. Cell information

Cell instance type	No. of cells	Area (μm^2)
Standard cells	175	1274.31
Combinational cells	170	1179.06
Sequential cells	5	95.26
Buffers	16	67.03
Inverters	113	778.28
Flipflops	5	95.26

Table 4. Utilization ratios

Cell/core ratio	75.43%
Cell/chip ratio	69.590
Cell utilization (non-fixed)	11.740
Cell utilization (non-fixed + fixed)	11.750
Blockage percentage	0.0100

Table 5. Chip and core information

	Width (μm)	Height (μm)	Area (μm^2)
Core	273	272.16	74299.06
Chip	300	300.00	90000.00

Table 6. Layer information

Name	Direction	Fat metal	Pitch (μm^2)	Spacing (μm^2)	Width (μm^2)
Metal 1	Horizontal	No	0.28	0.12	0.12
Metal 2	Vertical	No	0.28	0.14	0.14
Metal 3	Horizontal	No	0.28	0.14	0.14
Metal 4	Vertical	No	0.28	0.14	0.14
Metal 5	Horizontal	No	0.28	0.14	0.14
Metal 6	Vertical	No	0.28	0.14	0.14
Metal 7	Horizontal	No	0.28	0.14	0.14
Metal 8	Vertical	Yes	0.84	0.42	0.42
Metal 9	Horizontal	Yes	0.84	0.42	0.42

5. CONCLUSION

ASIC designing of Rademacher functions and Walsh functions is modeled and simulated in CMOS 90 nm CBIC technology. Maximum operating frequency for this design is found to be 40 Mhz. Leakage Power consumption is very low and it is feasible for systolic designs. Dynamic Power can also be reduced by using sequential cells instead of combinational cells, but due to complex arithmetic operations it is not possible. Switching Power of the design is also considered as the culprit for larger Dynamic Power. This design has been done as an Intellectual Property (IP). Designed IP can be used as the basic block for the High Level design of Walsh Transforms. Furthermore this design can also be used as the basic block for arbitrary signal generator.

6. ACKNOWLEDGEMENT

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