

## Inverse Sine Phase Detector Phase Locked Loop Associated with Modified Multi Band LC Quadrature Voltage Controlled Oscillator for Wireless Communication Systems at 0.9, 1.8, 2.4, 3.5 GHz

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**Abstract: Problem statement:** In this study and in consequence of the restricted performance of the multi standard wireless receiver utilizing the classical architectures, we proposed and presented a new architecture of multi band wireless receiver based on an Inverse Sine Phase Detector Phase Locked Loop (ISPDPLL) associated with modified multi band LC quadrature Voltage Controlled Oscillator (VCO), supporting GSM/DCS/DECT/Bluetooth/WiMax systems. **Approach:** To accomplish the multi standard receiving architecture at sufficiently good performance and at a low hardware cost, the proposed circuit, using an ISPDPLL associated with VCO based on switched capacitors utilizing a several numeric controlled capacitive branch and cross-coupled transistors, was implemented in 0.35  $\mu\text{m}$  CMOS technology and designed to yield quadrature output signals (I-Q) allowing to eliminate the dephasing block ( $90^\circ$ ) employed in a multi band Zero IF architecture receiver, that make the proposed architecture amenable for monolithic integration and 4G multi standard application. **Results:** This novel system presented high performance and good potentiality to cover perfectly the wireless multi standard receiving on the large band with the same transmission condition. **Conclusion/Recommendations:** The performance of this system was analyzed and demonstrated to have a minimum phase noise, a good Factor Of Merit (FOM) and wide tuning for these standard applications.

**Key words:** Wireless receiver architecture, ISPD PLL, multi band LC quadrature VCO, phase noise, tuning range, FOM

### INTRODUCTION

Phase Locked Loop (PLL) is used widely in the implementation of modern systems, particularly in the field of communication applications. But, This PLL, called classical PLL, presents many disadvantages and limitations due especially by the loop filter which causes many problems such as aliasing effect and the limitation of bandwidth because if the filter bandwidth is decreased, the capture process became slower, the capture range decreases and the lock up time increases. In the other hand, the aim problem for the standard PLL is the phase error/phase noise. Many studies are developed to reduce phase error and phase noise by the addition of feedback loops<sup>[1]</sup>. In this way, the standard PLL can be tuned by first designing the transient and steady state of a second-order PLL and then taking care of the working operation under steady frequency (third order) and frequency ramps (fourth order).

Those including eluded because it is very complex. Anything else, the conventional PLL stay to operate in a wide hold range with important phase error and higher phase noise's due to employ three loop filters. For thus, a new architecture of the PLL is proposed,

called Inverse Sine Phase Detector Phase Locked Loop (ISPDPLL). The ISPDPLL is a PLL structure without using any filters and the phase detector and the loop filter used generally in the standard PLL are replaced by a Inverse Sine Phase Detector (ISPD) including a track and Hold circuits (T/H), an inverse converter and a Voltage Controlled Oscillator (VCO)<sup>[2-4]</sup>. The suppressed filter in the ISPDPLL makes the system able to operate in a large band frequency without using any gain block and minimizes the lock up time of the circuit. The ISPD is the useful way to enhance the limitation of the locking range of the conventional PLL<sup>[2]</sup>. To accomplish the multi band receiving architecture (Fig. 1) at a low hardware cost, many propositions are presented based on:

- A PLL with two selectable ring VCOs or LC VCO or the accumulation MOS varactor followed by a divide by N and frequency selector (Fig. 2). A ring VCO<sup>[5]</sup> has a benefit of a wide tuning range and a drawback of a high phase noise to enable that is disqualified for most structures in modern RF transceivers. Accordingly, most investigations are focused on the LC VCO design. Owing to the

limited range of the variable capacitance of the varactor, the tuning range of CMOS LC VCOs is very small. Hence<sup>[6]</sup> proposed that the varactor was controlled by the DC potentials at both of its input terminals to enable the LC VCO yielding a wide tuning range. Fong<sup>[7]</sup> developed the accumulation MOS varactor to provide wide band tuning capability at a low supply voltage. However, many studies explore the tuning range of LC VCO but may not meet the multi band requirement

- An ISPDPLL multi band synthesizer with frequency calculator is proposed herein to achieve a low phase noise with a narrow tuning range for GSM / DCS and WiMax systems (Fig. 3). This multi band synthesizer using the ISPDPLL architecture associated with frequency calculator block responsible to generate all the frequency bands and three numeric controlled blocks which

control the band selection, the steps selection in the selected band and the variation of the step selected and that's why the different band are usually didn't have the same characteristics. The frequency calculator, which be conceived by a combination of a frequency operators like dividers and multipliers, allows to translate the frequency generated by the ISPDPLL to the frequency range of the desirable band. The step selection and the variation of the step selected was conceived by programmable dividers<sup>[8]</sup>. Owing to the limited covering range of the operators (doubler or divide by 2), the frequency range of the multi band wireless receiver and especially the tuning range of the VCO is very small. However, many studies explore the tuning range of VCO with a low phase noise, but may not meet the multi band requirement

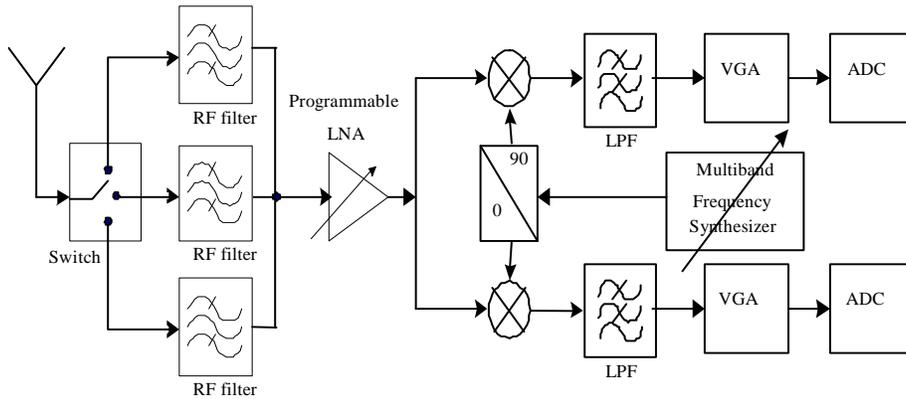


Fig. 1: Multi-band Zero IF architecture Receiver

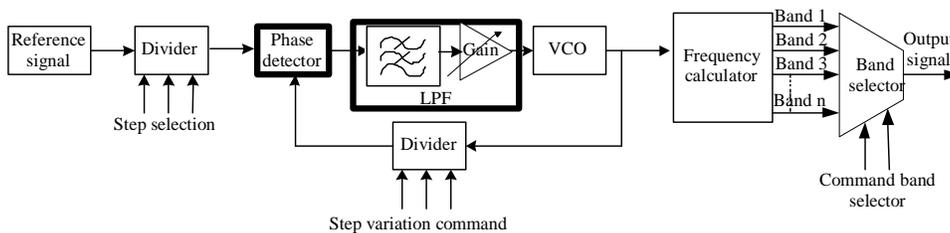


Fig. 2: Multi-band frequency synthesizer architecture based on standard PLL

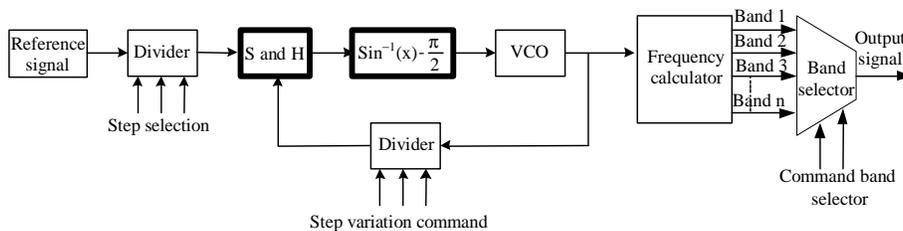


Fig. 3: Multi-band frequency synthesizer architecture based on ISPD PLL

To overcome this drawback, the ISPDPLL using the multi band LC quadrature VCO is proposed to achieve a wide tuning range with low phase noise/phase error and supporting many bands of the wireless communication. Improvements about the wireless receiver structure consist particularly to merge or to unit the dephasing block (90°), used generally in the multi band Zero IF architecture receiver, with the VCO allowing obtaining a unit cell called multi band LC quadrature VCO which associated with ISPDPLL.

**MATERIALS AND METHODS**

The aim of this research is to give a clear and concise exposition of the proposed system operating cycle. This provide sufficient detail to allow the work to be repeated by the others. In this research, we presented and described a detailed of the design of the novel synthesizer based on ISPDPLL associated with a modified multi band LC quadrature VCO to insist on an originality of the system and his performance.

**Synthesizer based on ISPDPLL associated with a modified multi band LC quadrature VCO:** To face the enormous demand of mobile multi media applications with a very high data rates, the 4G front-end transceiver needs a high performance which can be obtained mainly with an optimal architecture and a multi band VCO<sup>[9-11]</sup>; for thus, our idea, in this study, is to associate and to combine the ISPDPLL with a modified LC quadrature VCO for multi standards application. This modification reside to generate a separated bands (two bands for GSM900, one band for DCS1800-UMTS-Bluetooth and one band for WiMax: the VCO can cover the GSM standard at two separate bands (from 0.83-0.938 and 0.943-1 GHz) and the DCS/DECT/Bluetooth standards at one band (from 1.69-2.21 GHz) and the WiMax fixed standard also at one band (from 2.27-3.5 GHz) (Fig. 4) by using a several numeric controlled capacitive branches but not employed a binary weighted like<sup>[12-16]</sup>, to enlarge the frequency coverage according the desired band. Also, the main object, in this study, is to combine the advantages of the ISPDPLL<sup>[2]</sup> and the advantages of the multi band LC quadrature VCO<sup>[12]</sup> indeed to conceive a new architecture of multi band frequency synthesizer supporting GSM/DCS/UMTS/Bluetooth and WiMax. In the other hand, improvements, about the wireless receiver structure, using the new architecture, consist to merge or to unit the dephasing block with the LC quadrature VCO allowing to obtain a simples and a robustness circuit.

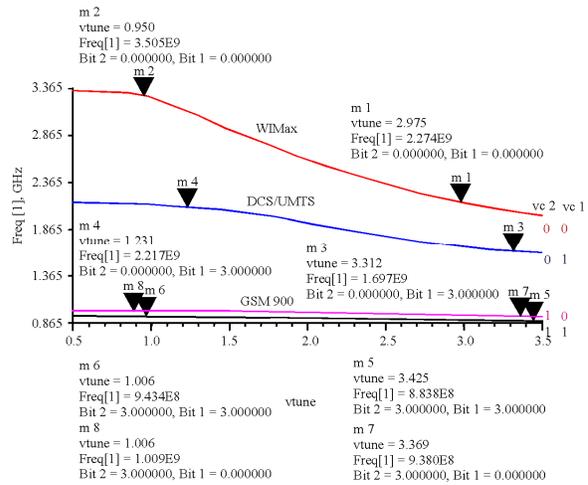


Fig. 4: Frequency oscillation vs. control voltage with switching combinations

**System description: ISPDPLL with LC quadrature VCO:** The proposed multi-band synthesizer using ISPD associated with multi band quadrature LC VCO and two digital controlled blocks which control the steps selection in the selected band and the variation of the step selected to make the synthesizer able to operate at different bands, is shown in Fig. 5. The system consists of ISPDPLL associated with a modified multi band LC quadrature VCO (LC QVCO).

Recall to the ISPDPLL is a PLL structure without using any filters and the phase detector and the loop filter used generally in the standard PLL are replaced by an Inverse Sine Phase Detector (ISPD) including a track and hold circuits, an inverse sine converter and a quadrature voltage controlled oscillator using the LC Tank (LC QVCO). The key assumptions and approximations of the ISPD involved with employing the mathematical description of the ISPD characteristic is already studied and designed in previous study<sup>[2,4]</sup> and given as:

$$f(x) = a(\sqrt{1+x} - \sqrt{1-x}) + c(x) \tag{1}$$

$$\text{With } c(x) = a_1 \times x + a_2 \times x^3$$

Where:

- a = 1.37
- a<sub>1</sub> = -0.37
- a<sub>2</sub> = -0.025

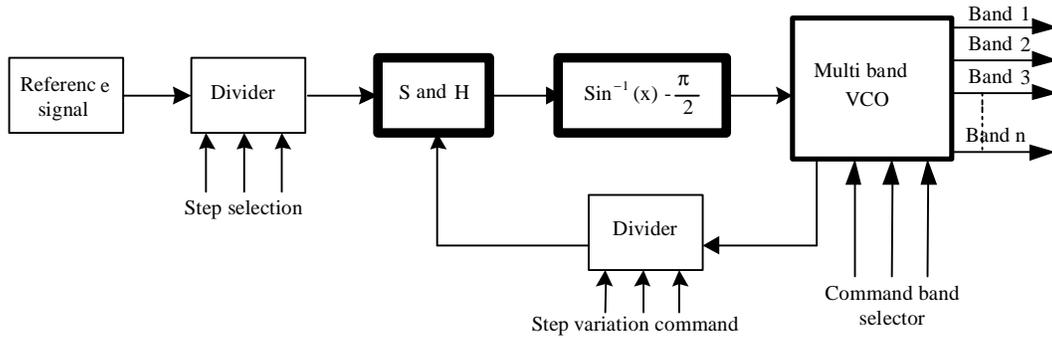


Fig. 5: Architecture of the proposed multi-band frequency synthesizer

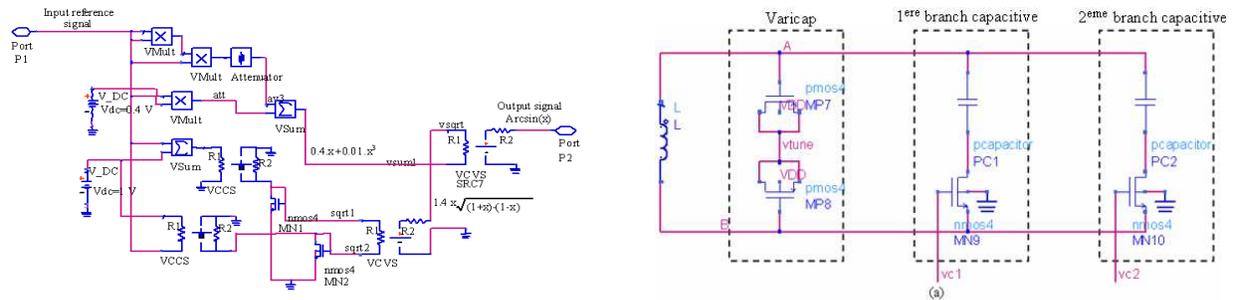


Fig. 6: ADS Simulation's diagram of the ISPD

Figure 6 shows the ADS simulation's diagram of the mathematical model of the ISPD. The suppressed filter in the ISPDPLL makes the synthesizer able to operate in a large band frequency without using any gain block and minimizes the lock up time of the circuit. This structure became completely integrated in the same wafer. The LC QVCO is designed to include cross-coupled transistors, switched capacitors, spiral inductors and varactor. The QVCO using LC tank is choose herein to achieve a low phase noise and low hardware cost for multi band applications. This QVCO can produce quadrature signals at different centred frequencies at a shared circuit block with the minimized overhead to support multi standards. According to these commonly used standards, the GSM, DCS-UMTS-bluetooth and WiMax have centred frequencies of 0.9, 1.8, 2.4 and 3.5 GHz. So, the conception of the proposed synthesizer is reduced to conceive and optimize the Multi-Band VCO which will determine the performance of the Local Oscillator circuit. The adaptation of the LC VCO architecture, for the GSM/DCS/DECT/Bluetooth and WiMax application, reside mainly on the determination of the number of switched capacitors branches needed to cover all the desired bands and the capacitors values. The modified LC quadrature VCO core consists of two cells (one in

Fig. 7: Transistor scheme of the multi band LCQVCO: (a): Resonator circuit; (b): Active circuit of each cell; (c): Equivalent scheme for the parasitic capacitance extraction

phase I, the second in Quadrature Q) and each cell is composed by cross-coupled transistors MP1, MP2, MN3 and MN4, to drive the LC tanks to generate full-swing output voltages, spiral inductor and a capacitance block to induce the required oscillation frequencies. The capacitance block is made by a varactor to assure the continuously variation of the frequency and a switched capacitors to assure the discrete variation of the bands (Fig. 7a, b and c).

**Design and analysis of the system:** In order to surpass the risk of the worst coverage of the minimal frequency band (GSM), we chose to divide the GSM coverage in two under-bands: The first can cover the uplink frequency range and the second can cover the downlink frequency range. Therefore, we need generate four bands: The first to cover the WiMax standards (2.5-3.5 GHz), the second to cover the DCS/DECT/Bluetooth standards (1.71-2.4 GHz), the third and the fourth to cover respectively the uplink and the downlink bands of the GSM standard. Besides, in order to optimize the LC QVCO architecture, both the varactor circuit, using of two capacitive branches is sufficient to cover four frequency bands, since the numeric command voltage «vc1» and "vc2" can take four numeric combinations, knowing that the low and the high logical states are respectively equivalent to 0V and 3V. Concerns Our conception's algorithm, we start with sizing the active circuit according to constraints of 0.35 μm process technology as supply voltage and the polarization current, after that we conceive the resonator circuit calibrated to cover the maximal frequency band (WiMax), then we pass to size the switching capacitances in order to assure the coverage of the minimal frequencies band (GSM).

To minimize the corner frequency of 1/f<sup>3</sup> phase noise, the active circuit (negative resistance) is indispensable to have a symmetrical CMOS structure with the identical Trans conductance on the PMOS and NMOS transistors<sup>[17]</sup>.

In the other hand, the grid Length (L) must be in general the smallest possible to decrease the thermal noise and to increase the transition frequency of the transistor (either L = 0.35 μm),

The main constraint imposed on the sizing of the varactor circuit, it is that it must allow the coverage of the largest frequency band, so, the capacitance variation of the varactor can determined by:

$$\Delta C_{var} \geq \max \left\{ \begin{array}{l} \Delta C_{WiMax}, \Delta C_{DCS/DECT/UMTS}, \\ \Delta C_{GSM,B1}, \Delta C_{GSM,B2} \end{array} \right\} \quad (2)$$

where, ΔC<sub>WiMax</sub> is the needed capacitance variation to cover the WiMax band; that is similar with ΔC<sub>DCS/DECT/UMTS</sub>, ΔC<sub>GSM,B1</sub> and ΔC<sub>GSM,B2</sub>.

The Inversion mode (I-MOS) and the accumulation mode (A-MOS) varactor structures present many advantages compared to the MOS structure like a wide and monotonous capacitance variation<sup>[16]</sup>, but the choice of the structure A-MOS involved replacing the p+ diffusions by a n+ diffusions, that impose a technology constraints. Then, in order to conceive a flexible and adaptable circuit by all technologies, it is amenable to use the I-MOS varicap structure.

In our application, we used a varactor structure composed by two PMOS transistors which each function's in I-MOS capacitance. This structure offers more stability opposite to the temperature effects<sup>[18]</sup>.

The sizing of the two branches capacitances is can deduced by calculating the maximal total capacitance value needed (C<sub>total,max</sub>), including the parasitic capacitances of the active circuit and the minimal total capacitance value needed (C<sub>total,min</sub>), including the parasitic capacitance of the active circuit (C<sub>MOS</sub>) and the varactor capacitance (C<sub>var</sub>):

$$C_{total} = C_{var} + C_{sw1} + C_{sw2} + C_{mos} \quad (3)$$

According to the Fig. 7c, the parasitic capacitance of the active circuit (CMOS) can be approximately by:

$$C_{mos} = C_{p,pol} + C_{n,pol} + C_{p,mos} + C_{n,mos} \quad (4)$$

With:

- C<sub>p,pol</sub> and C<sub>n,pol</sub> = The equivalent capacitance of the PMOS and NMOS polarization stages
- C<sub>p,MOS</sub> and C<sub>n,MOS</sub> = The equivalent capacitance of the differential CMOS structures

So, by determine the equivalent capacitance variation of the two branches, the sizing of the first branch must switch the VCO from the WiMax band to the DCS/DECT/UMTS band and the sizing of the second capacitance branch must switch the LC quadrature VCO from the DCS/DECT/UMTS band to the GSM band.

One of the main challenges of multi band synthesizer design based on ISPDPLL associated with modified LC quadrature VCO is to extend the narrow tuning range without degrading noise performance; for thus, we should minimized the corner frequency of 1/f<sup>3</sup> phase noise versus f<sub>offset</sub> allowing obtaining a lowest intersection frequency range between 1/f<sup>2</sup> and 1/f<sup>3</sup> (Δf<sub>1/f</sub><sup>3</sup>/f<sub>offset</sub> is neglected). In this case, the phase noise performance of the proposed multi band circuit is simulated, which integrates the following expression:

$$PN(f_{offset}) = 10 \log \left[ \frac{\alpha_N K_B T \Delta f}{P_{dis}} \times \left( 1 + \left( \frac{f_{osc}}{2Qf_{offset}} \right)^2 \right) \right] \quad (5)$$

Where:

- α<sub>N</sub> = The noise factor
- k<sub>B</sub> = Boltzmann's constant
- T = The absolute temperature
- P<sub>dis</sub> = The power dissipation at the resonator part
- Q = The quality factor
- f<sub>offset</sub> = The offset frequency

Table 1: Phase noise and fom simulated values of the proposed circuit

Bands	Frequency GHz	Phase noise @ 1 MHz	FOM @ 1 MHz
WiMax	2.3	-137 dBc	-196 dB
	3.5	-128 dBc	-186 dB
DCS/UMTS/...	1.7	-125 dBc	-189 dB
	2.1	-118 dBc	-187 dB
GSM	0.8	-122 dBc	-180 dB
	1.0	-119 dBc	-179 dB

In Eq. 5:

$$f_{osc} = [2\pi\sqrt{L(C_{var} + C_{sw1} + C_{sw2} + C_{MOS})}]^{-1} \quad (6)$$

With:

$C_{SW1/2}$  = The equivalent first and second cell capacitance value

$C_{var}$  = The varactor capacitance

Usually, Figure Of Merit for the VCO is defined as<sup>[7]</sup>:

$$FOM = PN(f_{offset}) + 10\log(P_{dc} / 1mW) - 20\log(f_{osc} / f_{offset}) \quad (7)$$

where,  $P_{DC}$  is the DC power consumption of the QVCO.

### RESULTS AND DISCUSSION

In this research, we was taken as application the Multi standard wireless receiver based on ISPDPLL associated with a modified multi band LC quadrature VCO. Then, we summarized the major results in relation to any hypotheses advanced in this study. Discussed these results and compared with the literature references.

To study the performance of the system suggested, we determine its phase noise, Figure Of Merit, lock up time, keep/capture range and tuning range, as well as the output spectrum at all standards according to several parameters such as resonator's components sizes. For the analysis, the circuit dissipates 10.3 mA from a 3V supply. The Inductor was set to 15 pf; the varactor, the first capacitive branch and the second capacitive branch for each cell were set to (200  $\mu\text{m}$  / 30  $\mu\text{m}$ ), (10 pf / 100  $\mu\text{m}$  / 10  $\mu\text{m}$ ) and (10 pf / 225  $\mu\text{m}$  / 30  $\mu\text{m}$ ). The phase noise and Figure Of Merit of the system for all standards were summarized in the Table 1. Table 1 shows the simulated values of phase noise and Factor Of Merit (FOM) (using Fong expression<sup>[7]</sup>) of the proposed circuit at 1MHz Offset frequency, at the different generated bands. As can be seen in these results, the best phase noise of the proposed multi band circuit is-137dBc at 2.3GHz and the best FOM is -196 dB. The phase noise at all standards is shown in Fig. 8a-e.

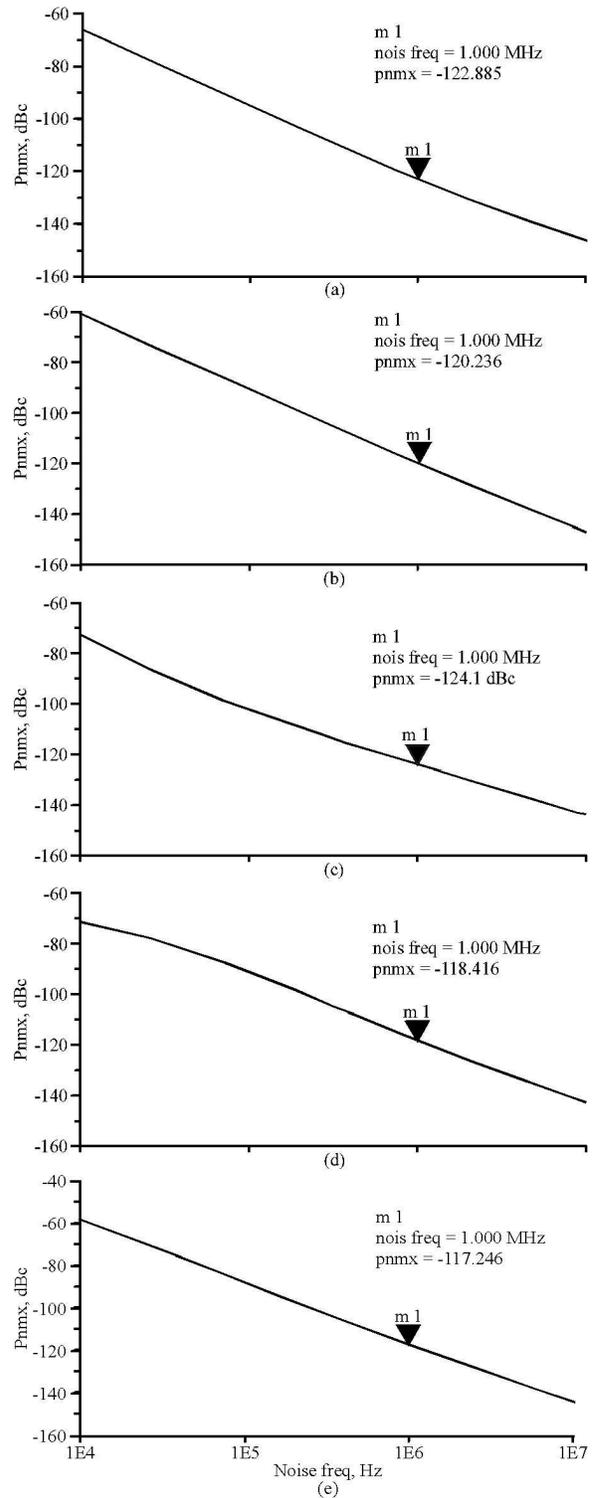


Fig. 8: Phase noise at 1 MHz offset frequency for different standards: (a): GSM; (b): DCS; (c): DECT; (d): Bluetooth and (e): WiMax

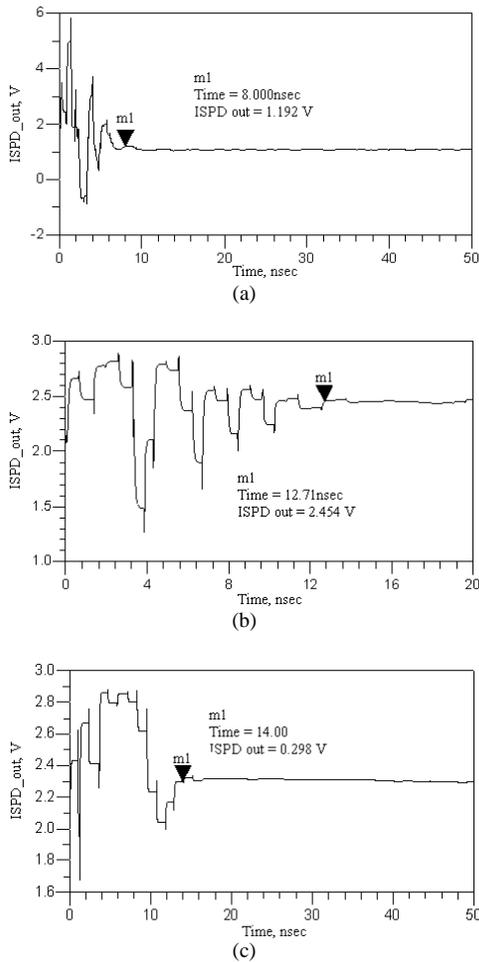


Fig. 9: Lock up time simulation of the circuit suggested at: (a): WiMax Band; (b): DCS band; (c): GSM band

To show the improvement made by the system suggested, we have carried out a comparative study with a system based on standard PLL and classical VCO. The results obtained show that the lock up time of the system suggested is better than the other systems. Knowing that the lock up time of the system based on the classical PLL/VCO is in order of 30 ns<sup>[19]</sup>, the lock up time of the system suggested at the WiMax band is 8ns (Fig. 9a-c). It is noticed that with configuration, the tuning range is wider than that of the system using standard PLL and classical VCO (78% versus 54%), which confirms that when the lock up time is better, the capture/keep range is larger and the tuning range is wide. According to Fig. 10a-c, the keep and capture range are higher than that of the system with standard PLL and classical VCO (0.7/1.4 GHz versus 100/ 380 MHz).

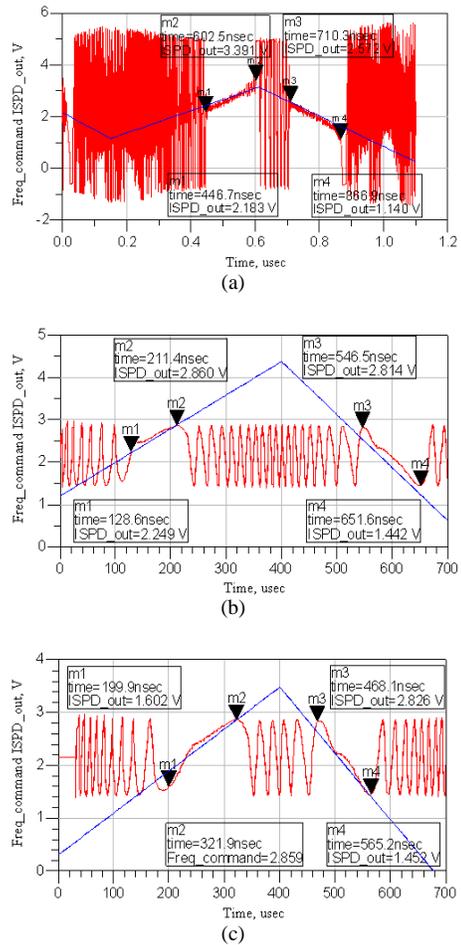


Fig. 10: Keep/capture range simulation of the proposed circuit applied in: (a): WiMax band, (b): GSM band, (c): Bluetooth band

We can also notice that the keep and capture ranges are the important characteristics of the frequency synthesizer, they describe its frequency performance. Generally, the keep range is limited by the linearity of the VCO, whereas the capture range depends on the gain and the speed of the synthesizer. To simulate the keep and capture ranges of the proposed synthesizer, we varied the frequency of the input reference signal by using another VCO controlled by the "Freq\_command" signal. According to the Table 1, we can conclude that the synthesizer, with its keep range, can cover the totality of all the desired bands (GSM/UMTS/DCS/DECT/WiMax) with a good and large capture range.

Figure 11 and 12 show the spectrum simulations of the proposed circuit respectively at minimal and maximal frequencies of each band. So, the simulation

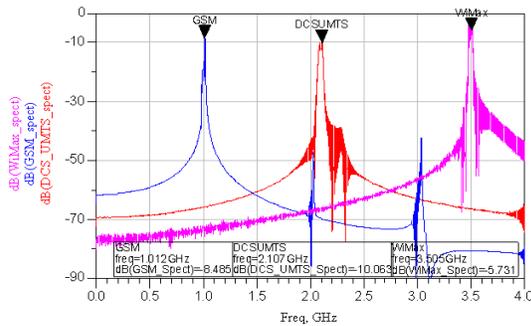


Fig. 11: Spectrum simulation of GSM/DCS-UMTS and WiMax at maximum frequency synthesized

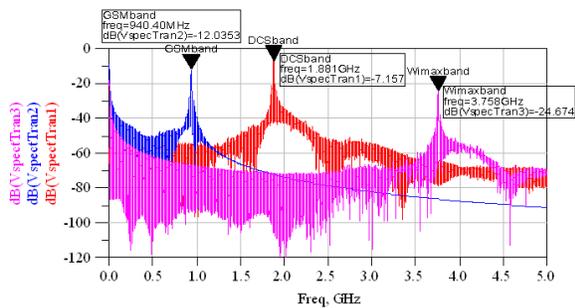


Fig. 12: Spectrum simulation of GSM/DCS/WiMax at minimum frequency synthesized

results show that by using the frequency synthesizer based on ISPD PLL without any filters and without any controlled gain block, we can cover the GSM/DCS/DECT/Bluetooth/WiMax bands with a good performance and a wide band frequency range, that make the proposed architecture receiver based on ISPD PLL amenable for monolithic integration and multi-band application.

### CONCLUSION

Due to the good performance of the modified multi-band LC quadrature VCO, the frequency synthesizer architecture based on ISPD PLL presented high performance and good potentiality to cover GSM/DCS/DECT/Bluetooth and WiMax bands. Moreover, the simplicity of this architecture allows saving area and power in favor of 4G programmable single chip-multimode-very high scale integration.

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