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Ultra Low Power Single Edge Triggered Delay Flip Flop Based Shift Registers Using 10-Nanometer Carbon Nano Tube Field Effect Transistor

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ABSTRACT

Carbon Nano Tube Field Effect Transistor is currently considered as promising successor of Metal Oxide Semiconductor Field Effect Transistor. The scaling down of the Metal Oxide Semiconductor device faced serious limits like short channel effect, tunnelling through gate oxide layer, associated leakage currents and power dissipation when its dimension shrink down to 22 nanometer range. Further scaling of Metal Oxide Semiconductor Field Effect Transistor will result in performance degradation. In this study, an ultra low power Single Edge Triggered Delay Flip Flop and shift registers are designed using 10 nanometre Carbon Nano Tube Field Effect Transistor. The Carbon Nano Tube Field Effect Transistor is an efficient device to supplant the current Complementary Metal Oxide Semiconductor technology for its excellent electrical properties. The high electron and hole mobility of semiconductor nano tubes, their compatibility with high k gate dielectrics, enhanced electrostatics, reduced short channel effects and ability to readily form metal ohmic contacts make these miniaturized structures an ideal material for high performance, nanoscale transistors. To evaluate the performance of Ultra low power Single Edge Triggered Delay Flip Flop and shift registers using 10 nanometer Carbon Nano Tube Field Effect Transistor technology, the results are depicted by analyzing average power, delay, power delay product, rise time and fall time using HSPICE at 1GHz operating frequency.

Keywords: Carbon Nano Tube Field Effect Transistor, Single Edge Triggered Delay Flip Flop, Shift Registers, Power, Power Delay Product, Rise Time, Fall Time

1. INTRODUCTION

The system on chip design will integrate hundreds of million transistors are dumped into one chip, whereas packaging and cooling both have a limited ability to eradicate the excess heat. So huge amount of heat should not be dissipated. Thus low power design is the need of today's integrated systems. The low power design is employed for the applications operated by batteries such as digital calculators, wrist watches, mobile phones, laptops, palmtops. Markovi *et al*. (2001) describes that the development of microelectronics takes time which is even lesser than the average life span of a human and yet it has seen as more than five generations. In early 60's itself the low density fabrication processes classified under small scale integration in which transistor count was limited to about 10. This rapidly gives way to medium scale integration in the late 60's when around 100 transistors could be placed on a single chip. It is important to improve the battery life as much as possible.

As the feature size of Complementary Metal Oxide Semiconductor technology process featured down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die.

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The increase in number of transistors will primarily increase the probability of reliability issues. Heat is one of the phenomenon packaging challenges in this era, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. The most vital prime mover of low power research and design is our convergence to a mobile society. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. This exhibits that low power tools and methodologies have to be developed and should be used in many number of applications.

Wang and Robinson (2010) describes that the current trends will primarily mandate low power design automation on a very large scale to satisfy the trends of power consumption of today's and future integrated chips. Sharma *et al*. (2009) describes that the power consumption of Very Large Scale Integrated design is given by generalized relation, $P = CV^2f$. Since power value is proportional to the square value of the voltage as per the relation, voltage reduction is the most prominent methodology to degrade power dissipation. However, the voltage reduction is results in threshold voltage reduction which bows to the exponential increase in leakage power By using single edge triggered flip-flops, the clock frequency could be degraded which in further cut in half while preserving the rate of data processing and operation. Using lower clock frequency might explore into large power savings in the clocked portions of a circuit, which includes the clock distribution network.

Power consumption is one of the critical parameter of Very Large Scale Integration circuit design. The sources of power consumption in a digital Complementary Metal Oxide Semiconductor circuits are:

- Short Circuit Power
- Static Power
- Capacitance Switching Power

1.1. Short Circuit Power

In digital Complementary Metal Oxide Semiconductor circuits, when both pull up and pull down network are in ON condition, then it exhibits a direct flow from V_{DD} to ground, which results in short circuit power dissipation. The short circuit energy for high to low transition and low to high transition are given by Equation (1 and 2):

$$E_{SCHL} = V_{DD}\int_0^{T_{CLK}} i\left(m_p\right)dt \tag{1}$$

$$E_{SCLH} = V_{DD}\int_{T_{CLK}}^{2T_{CLK}} i\left(m_n\right)dt \tag{2}$$

The short circuit power is given by Equation (3):

$$P_{SC} = \frac{\left(E_{SCHL} + E_{SCLH}\right)/_2}{T_{CLK}} \tag{3}$$

where, T_{clk} is the clock frequency.

1.2. Static Power

The static power of a Complementary Metal Oxide Semiconductor circuits is the power dissipated during steady state conditions. For nanoscale Very Large Scale Integration circuits, the leakage current is due to mainly for sub threshold voltage. Although dynamic power is dominant for technologies at 0.18µm and above, leakage (static) power consumption becomes another dominant factor for 0.13µm and below. One of the main contributors to static power consumption in Complementary Metal Oxide Semiconductor is sub-threshold leakage current i.e., the drain to source current when the gate voltage is smaller than the transistor threshold voltage.

Power consumption is dominated by leakage power dissipation when the device dimension brought down to sub-22 nm technology. The static power of a circuit could be found by measuring the leakage power during logic high and logic low output with V_{SS} as input and V_{DD} as input respectively.

1.3. Capacitance Switching Power

The power dissipation due to charging and discharging of the capacitance during transistor switching is said to be capacitance switching power. It falls under the category of dynamic power dissipation. It can be found by using the following energy relations Equation (4):

$$E_{Dyn\_LH} = E_{Total\_LH} - E_{SC\_LH} - E_{Static\_H} \tag{4}$$

Where Equation (5 and 6):

$$E_{Total\_LH} = V_{DD}\int_{T_{CLK}}^{2T_{CLK}} i\left(V_{DD}\right)dt \quad (5)$$

$$E_{Dyn\_HL} = E_{Total\_HL} - E_{SC\_HL} - E_{Static\_L} \quad (6)$$

Where Equation (7):

$$E_{Total\_HL} = V_{DD}\int_{0}^{T_{CLK}} i\left(V_{DD}\right)dt \quad (7)$$

Dynamic power due to capacitive switching can be measured by using (P_{Dyn}) Equation (8):

$$P_{Dyn} = \frac{\left(E_{dyn\_LH} + E_{dyn\_HL}\right)/_2}{T_{CLK}} \quad (8)$$

This study is organized as follows: Section II gives explanation about the proposed single edge triggered delay flip-flop, Section III explains the carbon nano tube field effect transistor and their specifications. The low power delay flip flop based Serial in serial out, serial in parallel out, parallel in serial out and parallel in parallel out shift registers are explained in section IV. Results for low power delay flip flop, serial in serial out, serial in parallel out, parallel in serial out and parallel in parallel out shift registers using 10 nm Carbon NanoTube field effect transistor model are depicted in section V and performance of low power delay flip flop, serial in serial out, serial in parallel out, parallel in serial out and parallel in parallel out shift registers using 10 nm carbon NanoTube field effect transistor model are evaluated in terms of average power, delay, power delay product, rise time and fall time in Section VI. Paper ends in Section VII with the conclusion.

2. PROPOSED LOW POWER SINGLE EDGE TRIGGERED D-FLIP FLOP

The proposed low power single edge triggered delay flip flop is designed as shown in **Fig. 1** using Khan *et al*. (2011) describes about Power Personal Computing 603 Flip flop and Mathan *et al*. (2013) describes about modified single edge triggered delay Flip flop, depicts such that it is efficient and reliable comparing all sorts of designs. It is basically a Master Slave flip flop structure and it consists of two data paths. A network restructuring low power technique is used to design the proposed low delay flip plop, by swapping the transistors both p-type metal oxide semiconductor and n-type metal oxide semiconductor which is present in regenerative feedback. When a clock is high, the p-type metal oxide semiconductor supersede switching activity and vice versa, in which this will act as a full sleep technique both in p-type metal oxide semiconductor and n-type semiconductor.

From this design, leakage current is reduced, that reduces leakage power consumption. Thus the proposed low power single edge triggered delay Flip Flop is free from threshold voltage loss problem of pass transistors. Thus the low power Single Edge Triggered delay Flip Flop has become more efficient in terms of area, power and speed which claim for better performance than conventional designs.

3. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Dang *et al*. (2006), describes that Carbon NanoTube Field Effect Transistors use semiconducting single wall Carbon Nano Tube to assemble electronic systems. Carbon Nano Tube Field Effect Transistors are having similar properties to that Metal Oxide Semiconductor Field Effect Transistors. A single wall Carbon Nanotubes consists of only one cylinder and the simple fabrication process of this device makes it a very promising alternative to today's that Metal Oxide Semiconductor Field Effect Transistors. Deng and Wong (2007) describes that a Single Wall Carbon Nanotubes can act as either a conductor or a semiconductor, which depends on the angle of the atom arrangement along the tube. Carbon is the most versatile element in the periodic table, owing to the type, Strength and number of bonds it can form with many different elements. The properties of carbon are a direct consequence of the placement of electrons around the nucleus of the atom. Carbon in the solid phase can exist in three allotropic forms: graphite, diamond and buckminsterfullerene. Diamond has a crystalline structure where each sp3 hybridized carbon atom is bonded to four others in a tetrahedral arrangement.

Graphite is made by layered planar sheets of sp2 hybridized carbon atoms bonded together in a hexagonal network. Buck minster fullerenes, or fullerenes, are the third allotrope of carbon and consist of a family of spheroid or cylindrical molecules with all the carbon atoms sp2 hybridized.

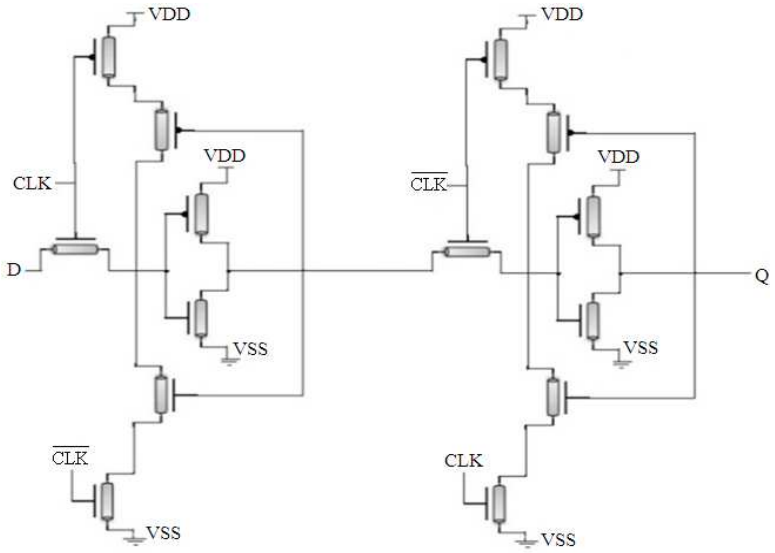

Fig. 1. Proposed Low Power single edge triggered delay flip flop using carbon NanoTube field effect transistor

Carbon nano tubes field effect transistors are used to replace the metal oxide field effect transistors for better reduction in power consumption. Silicon implied technology will reach its degradation in 2020 when the channel length of metal oxide field effect transistors is below 10 nm. For this comments, the semiconductor industry is looking for different materials and devices to integrate with the current silicon-based technology or maybe, in a long term future, even substitute it. Carbon nano tubes field effect transistors have predominant features and properties than metal oxide field effect transistors.

3.1. Carbon Nanotube Molecular Structure

The carbon nanotube is the forth stable structure of carbon after diamond and graphite and fullerene. An ideal nanotube can be thought of as a hexagonal network of carbon atoms that has been rolled up to make a seamless cylinder. Just a nanometer across, the cylinder can be tens microns of long, with half of a fullerene molecule. Guo *et al*. (2004) describes that a single wall nano tubes which are said as the fundamental cylindrical structure and these forms the building blocks of both multi-wall nanotubes and the ordered arrays of single-wall nano tubes called ropes as shown in **Fig. 2**.

3.2. Ballistic Carbon Nano Tubes Field Effect Transistors

Avouris *et al*. (2003) and Rahman *et al*. (2003) describes about three assumptions that are essential to consider for a Carbon nano tubes field effect transistor is in the ballistic regime, Carrier scattering events are quasi-suppressed in the intrinsic channel or carriers in the channel are free from scattering and all carriers propagating towards drain reach the drain without scattering back to the source. In this case, the carrier's transport is ballistic and in the ohmic zone, the drain current is expressed with elementary parameters without corresponding to the carrier mobility. This current depends on the channel length and is proportional to the channel width or nanotube diameter. Width of Carbon nano tube is defined by four different capacitors: drain, source, quantum and gate. Since gate capacitance is significantly higher than the three others, the total capacitance is upper limited by quantum capacitance. Carbon nano tubes field effect transistors operate in quantum capacitance limit. When gate capacitance is less than quantum capacitance, the charge at the beginning of the channel is nearly independent of the drain voltage as shown in **Fig. 3**.

When gate capacitance is greater than quantum capacitance, the charge at the beginning of the channel decreases when drain capacitance increases. In the quantum capacitance limit, instead of having the charge constant, the gate holds the nanotube potential constant, equal at the gate potential.

The scaling degrades of the Carbon nano tubes field effect transistors will be determined by 2D electrostatics and scattering and parasitic resistance will predominantly degrade the performance in practice. Nevertheless, the simple theory of the ideal Carbon nano tubes field effect transistors introduced here establishes for the first time upper performance limits and provides a useful guide for future work.

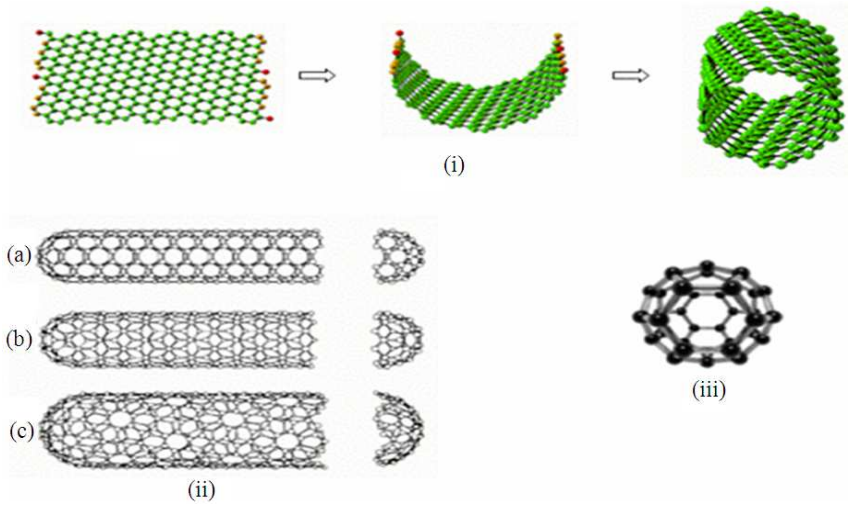

Fig. 2. (i) Formation Of Carbon Nanotube From A Graphite Sheet. (ii) Nanotube Structure With Fullerene 'cap'. (iii) A Fullerene (C60) Molecule

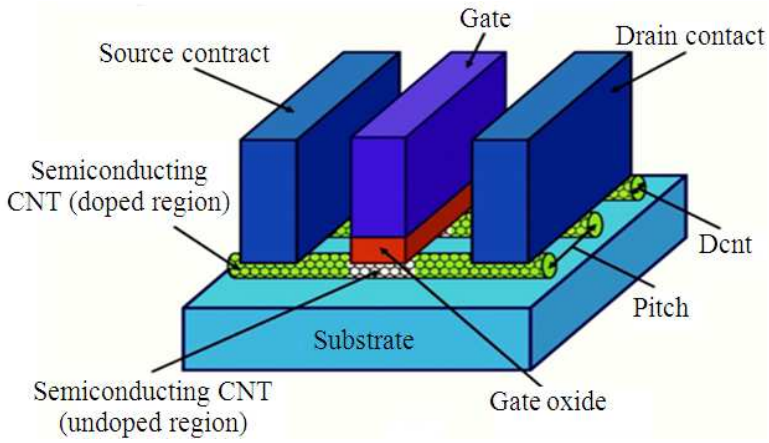

Fig. 3. Typical Carbon nano tubes field effect transistors device

The parameters which are designed as shown in **Table 1** are briefly explained as follows.

3.2.1.Channel Length

Markovi *et al*. (2001) describes the overall hike in current in our simulation can be proven by the physical explanation that the mean free path (A) is in general much longer than the channel length. The mean free path of intrinsic carbon nanotube modeled for elastic scattering is approximately equal to 200 nm, acoustic scattering is approximately equal to 500 nm and optical phonon scattering is approximately equal to 15 nm.

3.2.2. Pitch

Carbon nanotubes are grown or transferred to a substrate using a fixed spacing (pitch) prior to defining carbon nanotube-based gates and contacts. The channel region of carbon nanotube is undoped while the other regions of carbon nanotube are heavily doped, therefore they are acting as the source/drain extended region. So, the pitch must be carefully considered to avoid or minimize any additional steps such as electrical burning and selective etching to take care of the likely defects due to misaligned and mispositioned carbon nanotubes.

Table 1. Parameters of Carbon nano tubes field effect transistors model

Carbon nano tubes field effect transistors Model Parameters	10nm Ballistic Carbon nano tubes field effect transistors model
Physical channel length	10 nm
Diameter of the CNT	1.3502 nm
L_{SS}	10 nm
L_{DD}	10 nm
T_{OX}	2 nm
K_{OX}	16
Pitch	4 nm
Chiral vector	(17,0)
Ksub	3.9
lambda_ap	300 nm
lambda_op	15 nm
Phonon energy	0.16eV
Csub	23pF/m
Ccsd	0.0pF/m
Phi_M	4.6eV
Phi_S	4.5eV

3.2.3. Chirality Vector (n1, n2)

Theoretical studies have shown that a single-walled carbon nanotube can be either metallic or semiconducting depending on its chirality and diameter. (n,m) nano tubes with n = m are metallic, for n-m ≠ 3× integer, the nano tubes are semiconducting. For n-m = 3×integer, the nano tubes will be quasi-semiconducting with a small band gap. The sensitivity of carbon nanotube spectacular electrical properties on structural parameters opens up numerous opportunities in nano tube designs.

3.2.4. Diameter

The diameter of the carbon nanotube is found to be 1.3502 nm with a_{cc} = 0.144 nm (carbon-carbon bond length of graphene) and (17,0) for (n,m) chiral vector.

3.2.5. Thickness (tox)

In order to exhibit the ultimate scaling limit imposed by source-drain tunneling, very thin gate oxide is used to ensure excellent gate controlled electrostatics. Scaling of physical channel length down to 10 nm significantly increases the off current, but the on-off current ratio still exceeds 100, which can be acceptable for digital designs. From above considerations we took thickness to be 2 nm (tox = 2 nm).

4. SHIFT REGISTERS

In digital designs, a shift register is a cascade of flip flops, having the same clock each, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position. There are different types of shift registers are Serial in Serial out shift register, Serial in Parallel out shift register, Parallel in Parallel out shift register and Parallel in Serial out shift register.

Serial in serial out shift register accept data input serially on a single line and it gives the stored information on its output also in serial form. Carbon nanotube field effect transistor based serial in and serial out shift register design is shown in **Fig. 4**. Serial in parallel out shift register also accept data input in serial form. Once the input data is given, it may be either read off at each output simultaneously, or it can be shifted out and replaced. This configuration allows conversion from serial to parallel format. Carbon nanotube field effect transistor based Serial in parallel out shift register design is shown in **Fig. 5**.

Parallel in Serial out Shift Register configuration has the data input on lines d1 through d4 in parallel form. To write the data to the register, the write/shift control line should be held low. To shift the data, the write/shift control line is brought high and the registers are clocked. **Figure 6** arrangement shows Carbon nanotube field effect transistor based design of parallel in parallel out shift register. For parallel in parallel out shift register, all data bits occur as parallel outputs immediately following the simultaneous entry of the data bits with respect to clock. The circuit design of parallel in parallel out shift register constructed by Carbon nanotube field effect transistor based proposed single edge triggered flip flops and shown in **Fig. 7**.

5. TRANSISENT ANALYSIS

To evaluate the performance, low power delay flip flop based shift registers discussed in this study are designed using 10 nanometer technology in Carbon nanotube field effect transistor design. All simulations are carried out using HSPICE simulation tool at nominal conditions with 1GHz frequency range. The transient analysis of Proposed Low Power Delay Flip Flop based shift registers using Carbon nanotube field effect transistor are shown in **Fig. 8-12**.

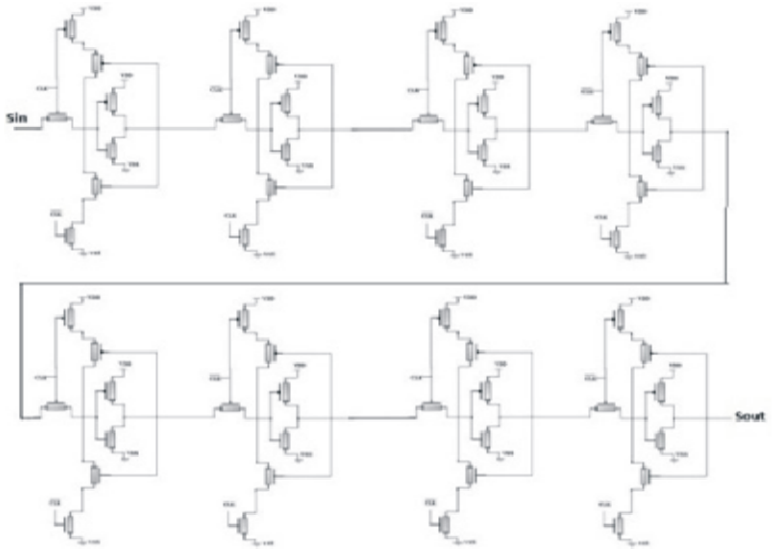

Fig. 4. Serial in-serial out shift register

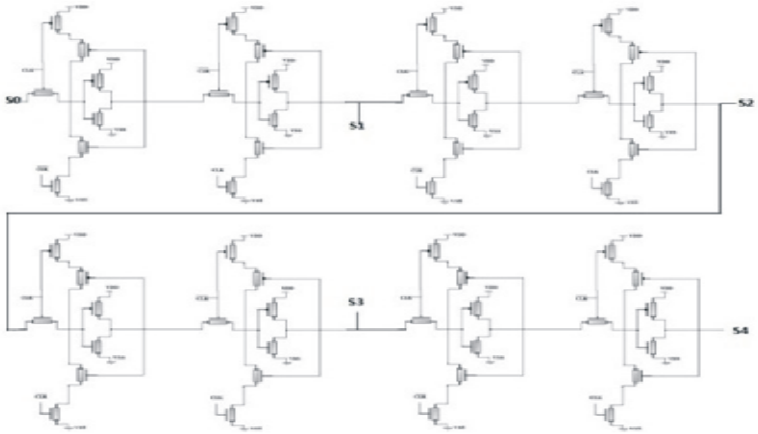

Fig. 5. Serial in-parallel out shift register

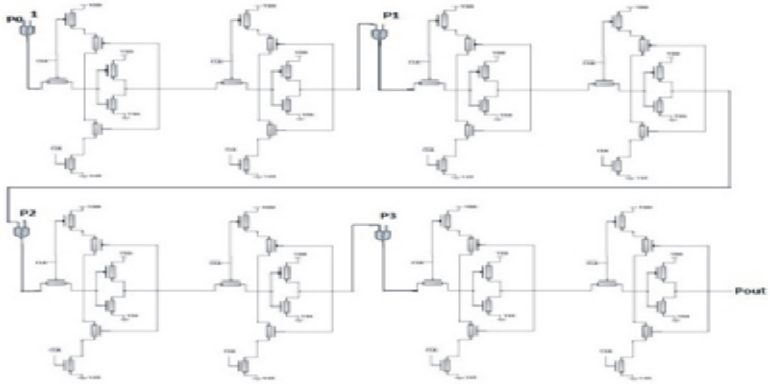

Fig. 6. Parallel in serial out shift register

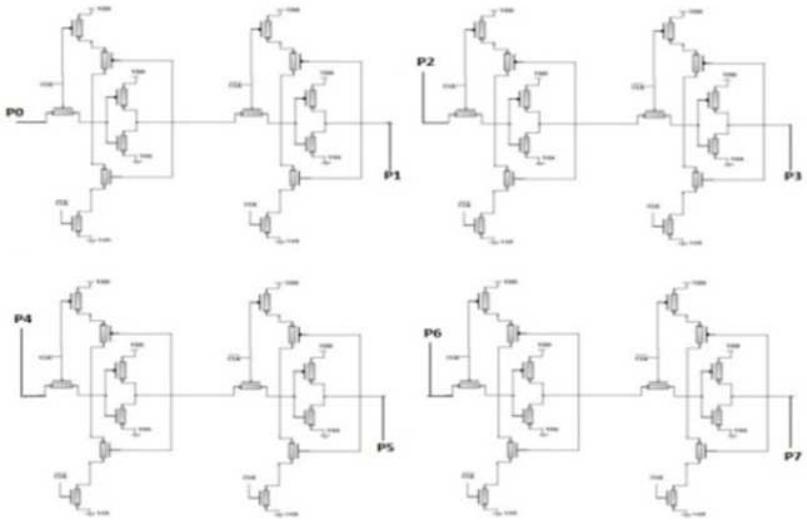

Fig. 7. Parallel in parallel out shift register

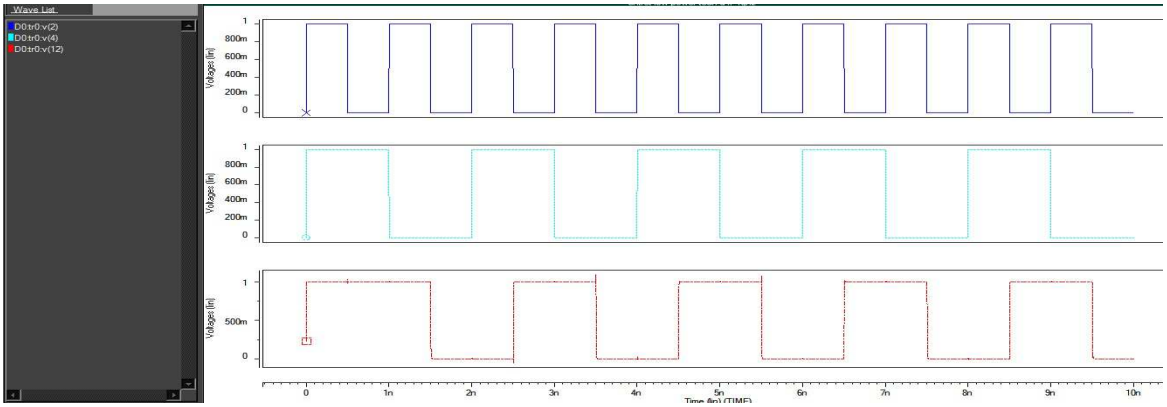

Fig. 8. Transient Analysis of Proposed Low Power delay flip flop using Carbon nanotube field effect transistor Design

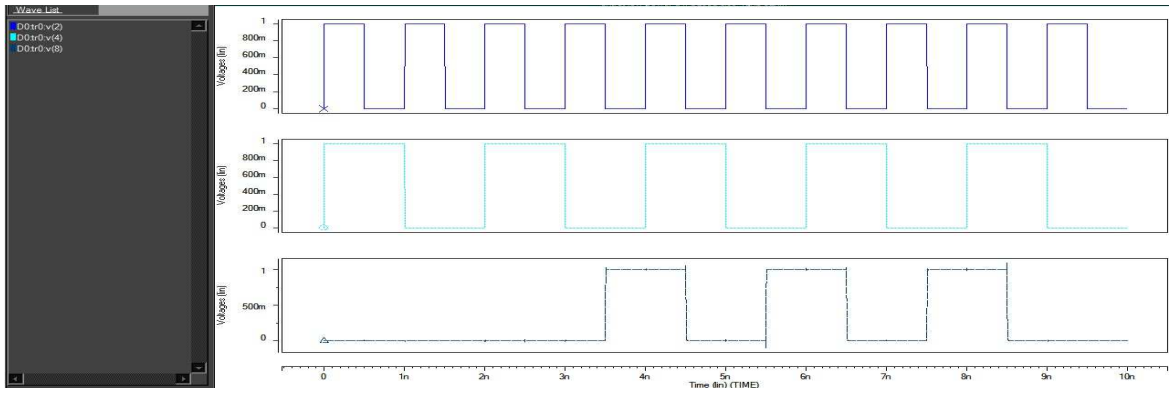

Fig. 9. Transient Analysis of Proposed Low Power delay flip flop based serial in serial out Shift Register using Carbon nanotube field effect transistor Design

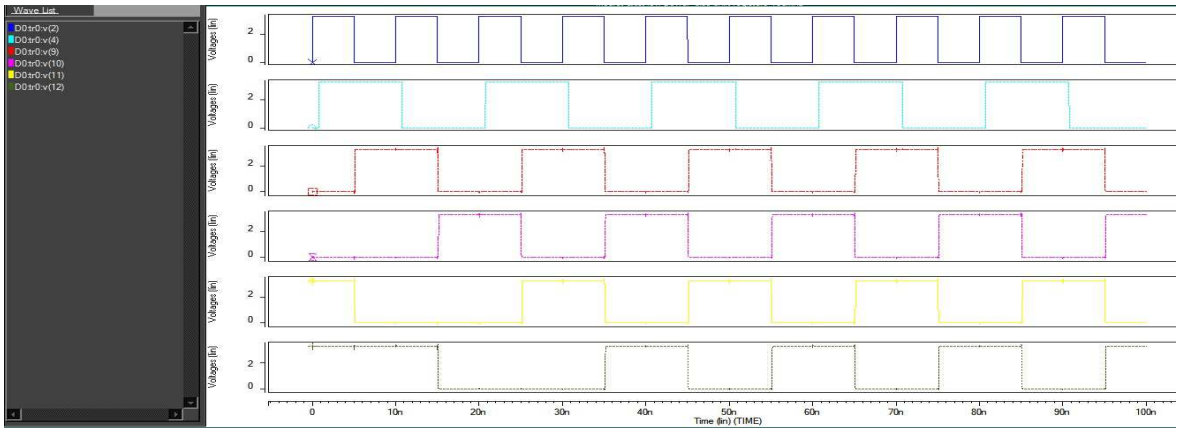

Fig. 10. Transient Analysis of Proposed Low Power delay flip flop based serial in parallel out Shift Register using Carbon nanotube field effect transistor Design

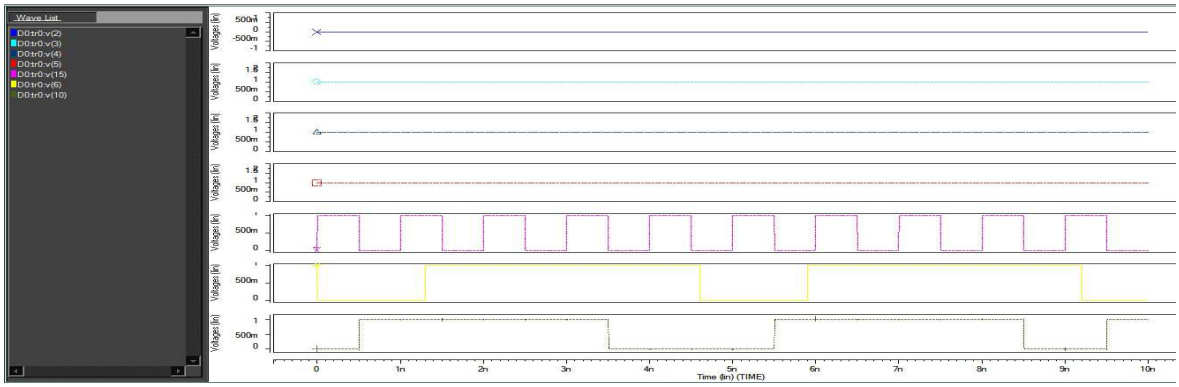

Fig. 11. Transient Analysis of Proposed Low Power delay flip flop based parallel in serial out Shift Register using Carbon nanotube field effect transistor Design

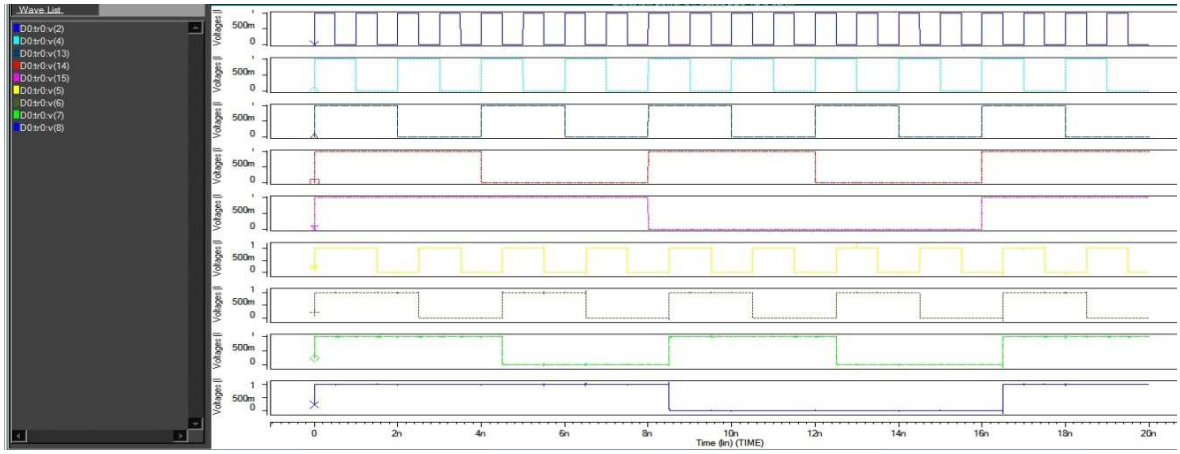

Fig. 12. Transient Analysis of Proposed Low Power delay flip flop based parallel in parallel out Shift Register using Carbon nanotube field effect transistor Design

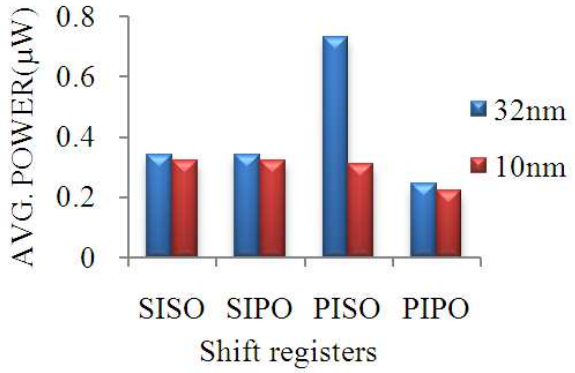

Fig. 13. Average power analysis of 32 and 10nm carbon nanotube field effect transistor design

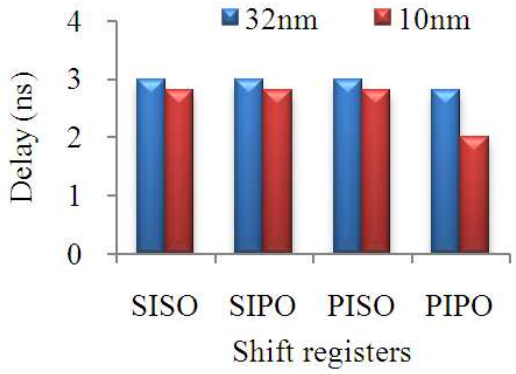

Fig. 14. Delay Analysis of 32 and 10nm Carbon nanotube field effect transistor design

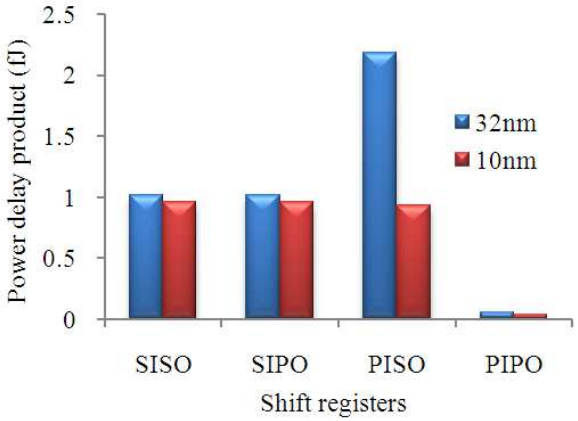

Fig. 15. Power Delay Product Analysis of 32 and 10nm Carbon nanotube field effect transistor design

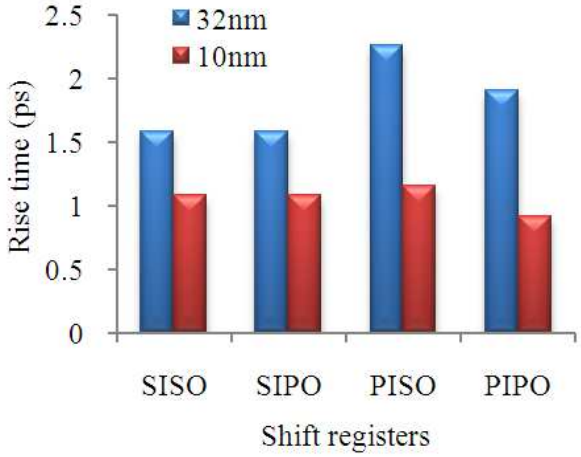

Fig. 16. Rise Time Analysis of 32 and 10nm Carbon nanotube field effect transistor design

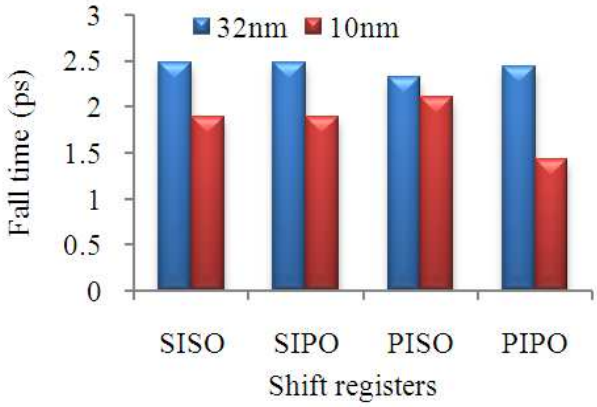

Fig. 17. Fall time analysis of 32 and 10nm Carbon nanotube field effect transistor design

Table 2. Operating frequency at 1 GHz using 32 nm technology in CNTFET design

Design	Avg Power (W)	Delay (s)	PDP (J)
D-FF	0.602e-07	3.173p	1.910e-19
SISO	0.034e-05	3.0029n	0.102e-14
SIPO	0.034e-05	3.674p	0.124e-17
		1.0033n	0.034e-14
		2.0040n	0.068e-14
		3.0029n	0.102e-14
PISO	0.234e-06	3.0080n	0.070e-14
PIPO	0.326e-06	3.214p	1.047e-18

Table 3. Operating frequency at 1 GHz using10 nm technology in CNTFET design

Design	AVG Power (W)	Delay (s)	PDP (J)
D-FF	0.564e-07	2.014p	1.127e-19
SISO	0.032e-05	3.0022n	0.096e-14
SIPO	0.032e-05	3.156p	0.1009e-17
		1.0032n	0.032e-14
		2.0028n	0.064e-14
		3.0022n	0.096e-14
PISO	0.228e-06	3.0072n	0.685e-15
PIPO	0.311e-06	2.990p	0.929e-18

Table 4. Rise time and fall time using 32nm technology in CNTFET design

Design	Rise time (s)	Fall time (s)
D-FF	1.472 p	2.414 p
SISO	1.582 p	2.471 p
SIPO	2.22 p	2.99 p
	2.6 p	2.91 p
	1.73 p	2.86 p
	1.582 p	2.471 p
PISO	2.267 p	2.32 p
PIPO	1.915 p	2.442 p

Table 5. Rise time and fall time using 10 nm technology in CNTFET design

Design	Rise time (s)	Fall time (s)
D-FF	1.132 p	1.214 p
SISO	1.082 p	1.891 p
SIPO	1.32 p	1.79 p
	2.198 p	1.718 p
	1.324 p	2.201 p
	1.082 p	1.891 p
PISO	1.162 p	2.109 p
PIPO	0.925 p	1.433 p

6. PERFORMANCE ANALYSIS

The performance of the low power Delay Flip Flop is evaluated by comparing the average power, delay and power delay product. In general, a power delay product based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency. The following **Table 2 and 3** furnished the performance parameters in 1GHz using 32nm and 10nm technology. **Table 4 and 5** depicts about the rise time and fall time responses using 32nm and 10nm technology.

Figure 13 shows the average power analysis of 32nm and 10nm carbon nanotube field effect transistor design

Figure 14 shows the delay analysis of 32nm and 10nm carbon nanotube field effect transistor design

Figure 15 shows the power delay product analysis of 32nm and 10nm carbon nanotube field effect transistor design.

Figure 16 and 17 shows the rise time and fall time analysis of 32nm and 10nm carbon nanotube field effect transistor design respectively.

7. CONCLUSION

Conventionally 32 nanometer Carbon nanotube field effect transistors are used as effective replacement of Metal Oxide Semiconductor Field Effect Transistors in digital circuits to overcome the scaling problems. However the performance of the digital circuits can be further improved if the channel length is reduced to 10nm. Main challenge in using 10 nanometer Carbon nanotube field effect transistors lies in the non-availability of its corresponding HSPICE model. Hence in this research work, an effective HSPICE model for 10 nanometer Carbon nanotube field effect transistor is developed and validated. Flip flop and Shift registers are simulated with the proposed Carbon nanotube field effect transistor model and the performances are compared with 32 nanometer Carbon nanotube field effect transistor. From the performance analysis, 10 nanometer Carbon nanotube field effect transistor design depicts low power consumption, less delay and improved power delay product than 32 nanometer Carbon nanotube field effect transistor design. However in the proposed model, gate capacitance of 10 nanometer Carbon nanotube field effect transistor is considered as that of 32 nanometer Carbon nanotube field effect transistor. Accuracy of Carbon nanotube field effect transistor model can be improved further by determining the optimal gate capacitance for 10 nanometer Carbon nanotube field effect transistor. Also the research work ended with simulation analysis. Fabrication of 10 nanometer Carbon nanotube field effect transistor and design of shift registers can be explored in future.

8. REFERENCES

Avouris, P., J. Appenzeller, R. Martel and S.J. Wind. 2003. Carbon nanotube electronics. Proc. IEEE, 91: 1772-84. DOI: 10.1109/JPROC.2003.818338

Dang, T., L. Anghel and R. Leveugle, 2006. CNFET basics and simulation. Proceedings of the International Conference on Design and Test of Integrated Systems in Nanoscale Technology, Sept. 05-07, IEEE Xplore Press, pp: 28-33. DOI: 10.1109/DTIS.2006.1708731

Deng, J. and H.S.P. Wong, 2007. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application-Part I: Model of the intrinsic channel region. IEEE Trans. Elect. Devic., 54: 3186-3194. DOI: 10.1109/TED.2007.909030

Guo, J., S. Datta and M. Lundstrom, 2004. A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors. IEEE Trans. Electr. Devic., 51: 172-177. DOI: 10.1109/TED.2003.821883

Khan, I.A., O.A. Shah and M.T. Beg, 2011. Analysis of different techniques for low power single edge triggered flip flops. Proceedings of the World Congress on Information and Communication Technologies, Dec. 11-14, IEEE Xplore Press, Mumbai, pp: 1363-1367. DOI: 10.1109/WICT.2011.6141447

Markovi, D., B. Nicolic and R. Borders, 2001. Analysis and design of low-energy flip-flops. Proceedings of the International Symposium on Low Power Electronics and Design, Aug. 06-07, ACM Press, New York, USA., pp: 52-55. DOI: 10.1145/383082.383093

Mathan, N., T. Ravi and V. Kannan, 2013. Low power single edge triggered D flip flop based shift registers using 32nm technology. Int. J. Eng. Res. Technol., 2: 1-5.

Rahman, A., J. Guo, S. Datta and M.S. Lundstrom, 2003. Theory of ballistic nanotransistors. IEEE Trans. Electr. Devic., 50: 1853-1864. DOI: 10.1109/TED.2003.815366

Sharma, M., A. Noor, S.C. Tiwari and K. Singh, 2009. An area and power efficient design of single edge triggered D-flip flop. Proceedings of the International Conference on Advances in Recent Technologies in Communication and Computing, Oct. 27-28, IEEE Xplore Press, Kottayam, Kerala, pp: 478-481. DOI 10.1109/ARTCom.2009.207

Wang, X. and W.H. Robinson, 2010. A low-power double edge-triggered flip-flop with transmission gates and clock gating. Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems, Aug. 1-4, IEEE Xplore Press, Seattle, WA., pp: 205-208. DOI: 10.1109/MWSCAS.2010.5548695