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Design of Multi-Valued Quaternary Based Analog-to-Digital Converter

A.H.M. Zahirul Alam, Wahab Adetunji Lawal,
Sheroz Khan and Muhammad Mahbubur Rashid
Department of Electrical and Computer Engineering, Faculty of Engineering,
International Islamic University Malaysia, Kuala Lumpur, Malaysia

Abstract: Problem statement: The design of multi-valued quaternary based Analog-to-Digital Converter (ADC) circuit was presented. The ADC generates multi-valued logic outputs rather than the conventional binary output system to overall reduction in circuit complexity and size. **Approach:** Design was implemented using pipeline ADC architecture and was simulated using model parameters based on standard 0.13 µm CMOS process. **Results:** Performance analysis of the design showed desirable performance parameters in terms of response, low power consumption, and a sampling rate of 10 MHz at a supply voltage of 1.3V was achieved. **Conclusion/Recommendations:** The ADC design was suitable for the needs of mixed-signal integrated circuit design and can be implemented as a conversion circuit for systems based on multiple-valued logic design.

Key words: Analog to digital converter, multi valued, quaternary, pipeline ADC

INTRODUCTION

The era of digital electronics has been relying for long on the use of binary logic in the representation of signals, analog and digital alike. This involves representing signals in a format using two discrete levels corresponding to logic '0' and logic '1'. In an attempt to achieve more efficient and advanced realizations of electronic systems, binary logic implementation has witnessed various advancements leading of course to its present level of sophistication and complexity[1]. However, major issues such as the problem of components' interconnect and increasing chip density still pose major threats to the continued development of fabricating large scale binary integrated systems and implementation in Very Large Scale Integration (VLSI). With the ongoing trend of incorporating more functions and features into a single chip, the chip density is greatly increased, likewise, the number of interconnects required to transfer information within the chip and to communicate with other external devices or chips are greatly increased to the extent of risking the performance of the chip to be mostly dominated by the wirings rather than the actual number of devices fabricated on chip[2,3]. The threats posed by these limitations can be greatly reduced or compensated if digital signals are implemented in more than two discrete logic levels called higher radix representation such as in Multi-Valued Logic design approach.

Multiple Valued Logic (MVL) design approach, unlike the conventional binary logic approach, involves the use of more than two discrete logic levels ('0' and '1') for representation of a digital signal. The theoretical advantages digital systems designed with multi-valued logic approach include the abilities such as embedding of greater information content or reducing the number of gates required to implement logic functions as well as reducing the number of data interconnect lines within and in between the chips when it comes to in IC fabrication and design while improving the overall performance of the system[4-7]. However, these advantages can only be achieved through efficient circuit realizations of MVL building blocks. This work, in line with the increasing demand for efficient data conversion circuits in mixed-signals and System-On-Chip (SOC) design proposes an analog-to-digital converter circuit with multi-valued outputs rather than binary output. Such circuits will be intended for being used in the future MVL design systems, enabling them to communicate with external devices and systems for larger data contents and reducing usage of chips space. The remaining sections of this paper discuss the architecture for the proposed ADC design as well as presentation of results of the design and performance analysis of the proposed architecture.

Corresponding Author: A.H.M. Zahirul Alam, Department of Electrical and Computer Engineering, Faculty of Engineering, International Islamic University Malaysia, Kuala Lumpur, Malaysia

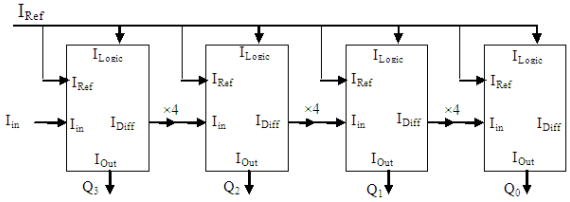

Fig. 1: Proposed ADC architecture

Proposed ADC architecture: The proposed design implements current mode pipeline ADC architecture to convert analog signals into quaternary (radix-4) MVL values. The configuration for a 4 digit resolution Analog-to-Digital Converter (ADC) of the design is as shown in Fig. 1. The conversion process involves using cascaded levels of comparator cells with the output of each cell and its position in the series representing a digit with its appropriate weight of the digitized output. The number of comparator cells defines the resolution of the converter. The inputs to the comparator cell are the analog input current to be digitized, I_{in} and the reference current, I_{Ref}. The reference current used here is equivalent to the current value of a single logic level, I_{Logic}. The comparator block produces an output of discretized current levels I_{Out} which are multiples of the logic value current, I_{Logic}. The current output level, I_{Out} depends on how large the input current, Iin is in comparison to multiples of the reference current I_{Ref}. The comparator cell is also designed to produce an output current, I_{Diff} which is the difference between the analog input current Iin and the output current level I_{Out}. The current difference output, I_{Diff} is used in facilitating the cascading of comparator cells. For I_{Diff} to be used as an input to the next input stage, it has to be scaled by a factor of four since the whole current input range has been discritized to four output levels. So the inputs to the next comparator cell will be four times I_{Diff} in place of the analog input current, Iin and the reference current I_{Ref} will be retained from the preceding stage. The whole process is repeated and hence the input currents for each successive stage 'i' of the comparator cell with the reference current, I_{Refi} and the input current I_{ini} is defined by the relation:

$$I_{ini} = 4*(I_{ini-1}-I_{Outi-1}) \quad (1)$$

where, I_{ini-1} and I_{Outi-1} are current input and current difference output of the preceding stage of comparator blocks.

MATERIALS AND METHODS

Figure 2 shows the schematic of a comparator cell. The working principle of the comparator cell can be explained as follows; the analog input current, I_{in} is compared with twice the reference current I_{Ref}, this determines if the Iin is within the upper or lower half of the full conversion current range. The comparator used here is a cascode current mirror comparator. The result of the comparison controls a MOS switch thus allowing or disallowing the flow to the output of a current two times the logic level current, I_{Logic}. This means that if the input current, I_{in}, is greater than half the full scale current range (which is equivalent to two times I_{Ref}), the current value which is two times the logic current level will be allowed to flow to the output. This operation generates two discrete current output levels with respect to the analog input current, I_{in}. In order to obtain the remaining two higher output levels, the difference of between $2*I_{Ref}$ and I_{in} is compared with I_{Ref} to decide on the more precise level in which the input current can be judged to be within the upper half or lower half of the full scale current range. If Iin is less than $2*I_{Ref}$, the subtraction will not be needed and Iin is simply compared with I_{Ref}. However if I_{in} is greater than $2*I_{Ref}$, then the difference of I_{in}-$2*I_{Ref}$ will be compared with I_{Ref} instead. A MOS switch is turned on/off in the cases of which one of the two options on subtraction is ultimately necessary. The result of this comparison will also control a MOS switch that allows or disallows the flow of the logic current level, I_{Logic} to the output. Hence an output current of four possible discrete levels is obtained by adding the resulting current that has been allowed/disallowed based on the outcome of the preceding two comparisons for use in the succeeding stage in the cell series. This output current defines which quarter of the full scale current range that the analog input current Iin falls in. Note that the value of I_{Ref} is the same as I_{Logic}. In the circuit in Fig. 2, inverters have been used to strengthen the signals obtained from the two comparison stages before it is passed on to the MOS switch. In order to obtain the I_{Diff} output of the comparison block, both the input current, Iin and output current I_{Out} are mirrored and subtracted from each other. Due to the differencing technique employed in determining the output levels for a comparator cell, there is a prospect in extending the design of the comparator block for generating higher discrete output current levels.

The proposed ADC circuit has been simulated using the model parameters of a standard 0.13 µm CMOS process. The length for the CMOS device is chosen to 0.35 µm to achieve higher current gains form the current mirrors at all cascaded levels. A logic level current is chosen to be multiples of 1 µA pending a level as well as a stage selection of a comparator cell.

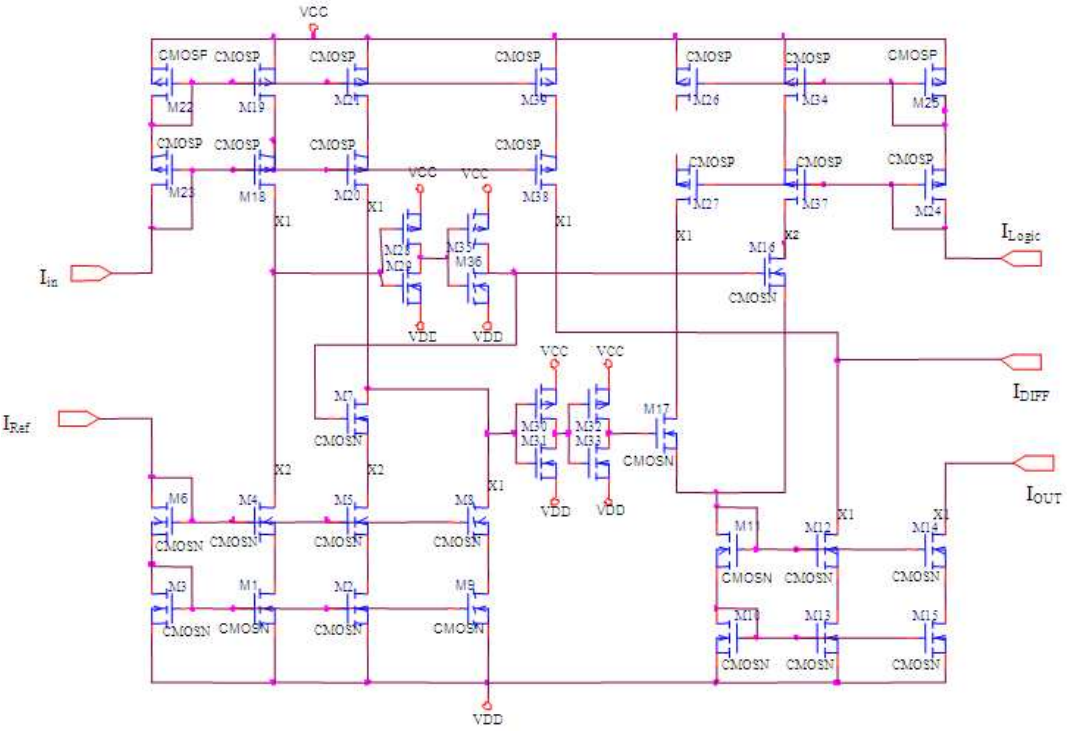

Fig. 2: Schematic for comparator cell

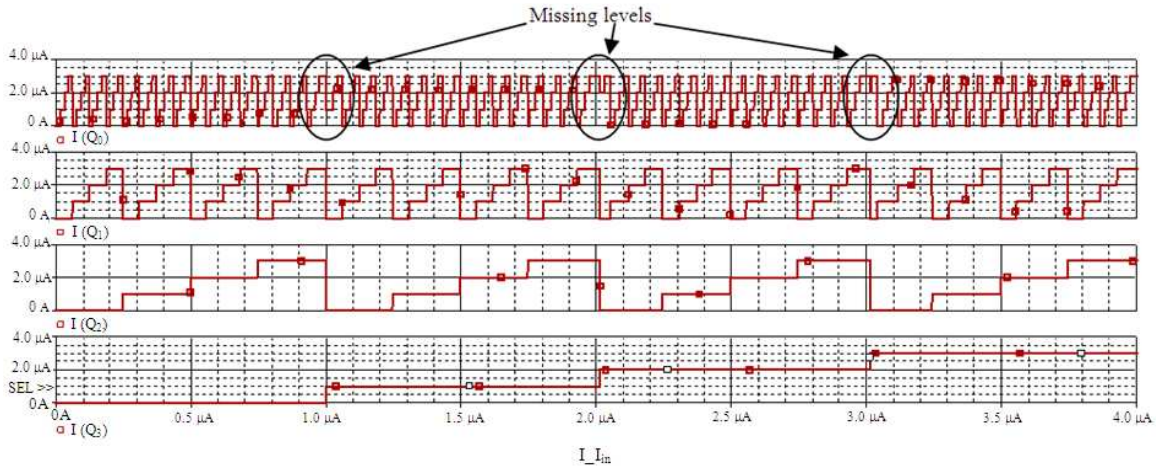

Fig. 3: Full scale transition

RESULTS

Figure 3 shows the digital current output resulting from a full-scale analog input current that is varying from 0-4 µA for up to four conversion stages realizing a four digit output. The Fig. 3 shows that there are some missing levels at the forth output digit.

The error plots from the reconstructed signal using both there and four conversion stages are also shown in Fig. 4. The reconstructed signal for the three-stage conversion is measured to have a maximum quantization error of 72.91 nA (equivalent to 1.2 times an LSB) while that of the four-stage conversion has a maximum error of 32.9 nA (equivalent to 2.1 times an LSB) at intervals with missing levels and a maximum of 12.46 nA (0.8 LSB) at other intervals.

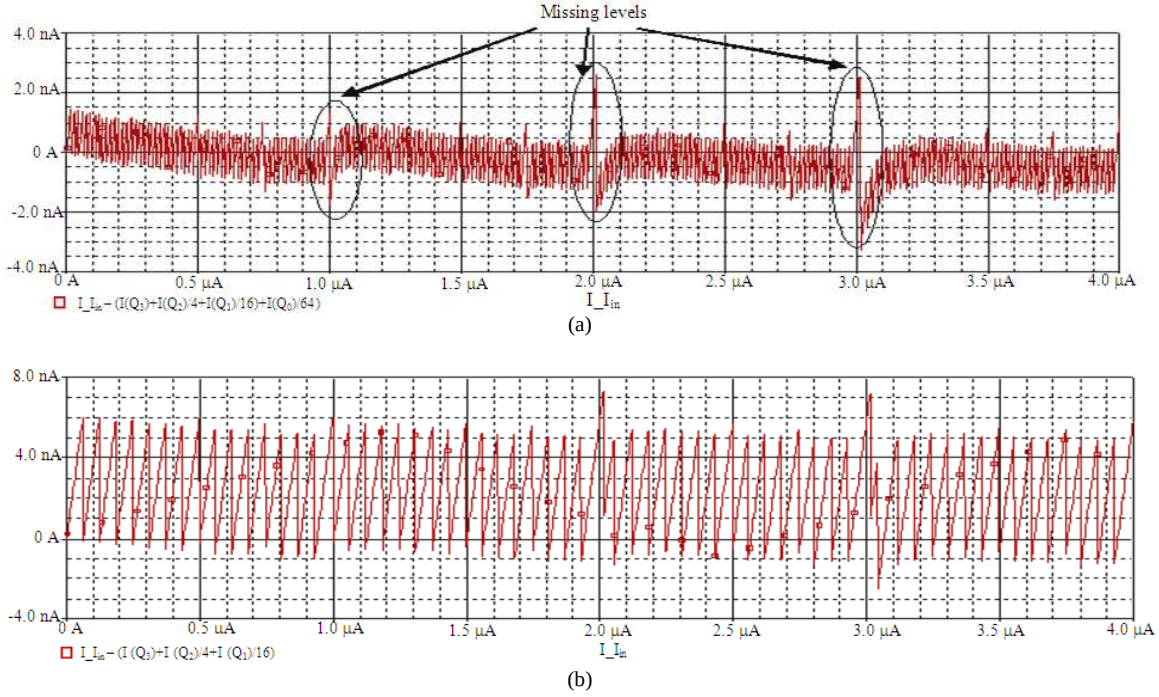

Fig. 4: (a): Four conversion stage error plot; (b): Three conversion stage error plot

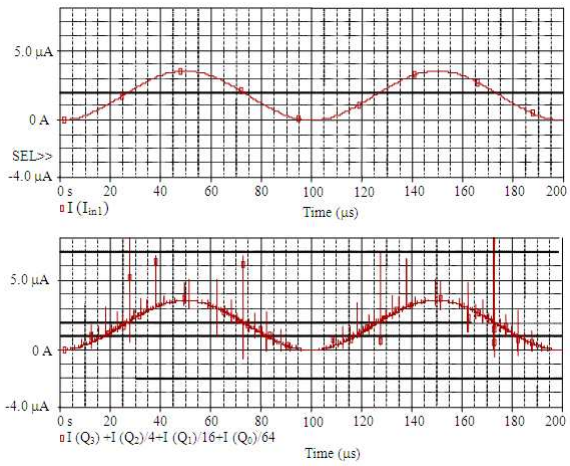

Fig. 5: Sinusoidal wave input test

The error is seen to be exaggerated beyond the code width at regions with missing levels. For a design with an output of three quaternary digits within the range of 0 to 4 µA, there are 4^3 (64) possible output states with a code width of 62.5 nA between each interval while a design with four quaternary digits will have 4^4 (256) possible output states with a code width of 15.625 nA.

A sinusoidal wave input test is performed for judging the performance of the ADC and a reconstructed wave form can be seen to synthesize closely the input wave with a couple of glitches as shown in Fig. 5.

DISCUSSION

The error propagated through the stages of the conversion process as shown in Fig. 3 due to inaccuracies in the current mirroring technique and those as a result of comparison and subtraction processes. The missing levels are noted to have occurred at intervals that require transitions form lower-to-higher position logic for all output digits. Missing levels are however not present at position of a third output digit.

The advantage of using multi-valued logic circuit can be noted here as a total of eight conversion stages will be needed to achieve a 256 level resolution using binary logic while the same resolution can be easily achieved in four stages using quaternary logic. Simulation results further show that the ADC has a maximum rise time of approximately 1.9 ns at the MSB position and 11 ns at the LSB position. The sampling frequency of the ADC is 10 MHz at a power supply voltage of 1.3 V and the measured average power dissipated is also 153.93 µW for the thee-stage conversion and 791.4 µW for the four-stage conversion.

Table 1: Performance for three and four conversion stages

	Three pipeline stages	Four pipeline stages
Technology	Standard 0.13 μm CMOS	Standard 0.13 μm CMOS
Resolution	3 digits-64 levels	4 digits-256 levels
Logic value	1 μA	1 μA
Code width	62.5 nA (1.56% full scale)	15.625 nA (0.39% full scale)
Rise time @ LSB	1.314 ns	11 ns
INL	< 0.62 LSB (0.98% full scale)	<2LSB (0.78% full scale)
DNL	< 0.65LSB (1% full scale)	<1.4LSB (0.56% full scale)
Sampling rate	10 MHz	10 MHz
Power supply	1.3 V	1.3V
Power consumption	153.93 μW	791.4 μW

This is considered to be quite low and satisfactory compared to other ADC designs. Table 1 shows a performance comparison for the three-stage and the four-stage ADC conversion stages using the proposed design.

The glitches as shown in Fig. 5 can be removed by using filters which are normally part of the analog-to-digital conversion process. Pre-amplification and post-amplification circuits might also be necessary to bring the input current to within the transition range of the ADC design and to set output logic level to the desired current levels for the application circuitry. This design is currently limited by the error propagated through the conversion stages which in turn results in missing levels at the fourth conversion stage, the design can be further improved by implementing more advanced and accurate current mirrors at the cost of increased size and larger power consumption.

CONCLUSION

A new ADC design has been proposed in this research. The design implements multiple valued logic output instead of the conventional binary output. The use of multiple-valued logic outputs for ADC design offers the possibility of an overall reduction in circuit complexity and size. A performance analysis test on the design using the model parameters for a 0.13 μm standard CMOS process shows the design obtaining desirable parameters in terms of rise time, speed, power consumption and extensibility of design. However, the error propagated through the conversion stages from the inaccuracies in the mirroring technique results in a few missing output levels. Being modular and cellular in nature, study is in progress for extending it to a higher-radix ADC design with reduced output errors and better performance parameters. The main purpose for designing an analog-to-digital converter with higher radix output is to generate MVL signals. Such signals will be needed by MVL based devices compatible to be interfaced to external devices and systems alike.

REFERENCES

1. Dubrova, N., 1999. Multiple-valued logic in VLSI: Challenges and opportunities. Proceedings of the NORCHIP'99, Nov. 8-9, Oslo, Norway, pp: 340-350. http://biblioteca.universia.net/ficha.do?id=41696096
2. Kameyama, M., 1990. Toward the age of beyond-binary electronics and systems. Proceedings of the Twentieth International Symposium on Multiple-Valued Logic, May 23-25, IEEE Xplore Press, Charlotte, NC., USA., pp: 162-166. DOI: 10.1109/ISMVL.1990.122613
3. Oklobdzija V.G., 2008. The Computer Engineering Handbook: Digital Design and Fabrication. 2nd Edn., CRC Press, Taylor and Francis Group, LLC., ISBN: 9780849386022, pp: 656.
4. Dornajafi, M., S.E. Watkins, B. Cooper and M.R. Bales, 2008. Performance of a quaternary logic design. Proceedings of the 2008 IEEE Region 5 Conference, Apr. 17-20, IEEE Xplore Press, Kansas City, MO., pp: 1-6. DOI: 10.1109/TPSD.2008.4562722
5. Shirahama, H. and T. Hanyu, 2008. Design of high-performance quaternary adders based on output-generator sharing. Proceedings of the 38th International Symposium on Multiple Valued Logic, May 22-24, IEEE Xplore Press, Dallas, TX., pp: 8-13. DOI: 10.1109/ISMVL.2008.11
6. Mochizuki, A., T. Kitamura, H. Shirahama and T. Hanyu, 2006. Design of a microprocessor datapath using four-valued differential-pair circuits. Proceedings of the 36th International Symposium on Multiple-Valued Logic, May 17-20, IEEE Computer Society, Washington DC., USA., pp: 14-14. http://portal.acm.org/citation.cfm?id=1130212
7. Temel, T. and A. Morgul, 2002. Multi-valued logic function implementation with novel current-mode logic gates. Proceedings of the IEEE International Symposium on Circuits and Systems, (ISCAS'02), IEEE Xplore Press, USA., pp: 881-884. DOI: 10.1109/ISCAS.2002.1009982