American Journal of Applied Sciences 5 (5): 605-609, 2008 ISSN 1546-9239 © 2008 Science Publications

Atomic Layer Epitaxial Growth of Gaas on Porous Silicon Substrate

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Abstract: GaAs thin film has been grown on porous silicon by metal organic chemical vapour deposition (MOCVD) for different growth temperatures using atomic layer epitaxy (ALE) technique. The morphology of GaAs layer was investigated by atomic force microscopy (AFM). The effect of growth temperature is studied using photoluminescence measurements (PL). The photoluminescence spectra revealed a dissymmetry form toward high energies attributed to strain effect resulting from the lattice mismatch between GaAs and porous Si substrate.

Keywords: GaAs, ALE technique, porous silicon, photoluminescence

INTRODUCTION

The heteroepitaxy growth of GaAs on Si and porous Si substrates has received great interest due to its potential for the monolithic integration of GaAs, Si and hybrid devices that combines the advantage of each material. However, the major problems are the large density of misfit dislocations and the threading defects resulting from the lattice mismatch (4, 2 %) and from the strong difference of the thermal expansion coefficient (240%) between GaAs and Si. The most important challenge is to obtain GaAs layers on Si with quality comparable to that on GaAs substrate. Several techniques have been proposed to obtain GaAs film on Si with the reduction of dislocation density such as the insertion of strained-layer superlattice (SLS)^[1] as buffer layer, the thermal annealing process^[2], the thermal cycle growth^[3] and the low-temperature growth^[4]. The porous silicon (PSi) has been investigated as a new material for microelectronic devices. The extensive studies have been devoted to the application of PSi in the electric isolation of integrated devices like insulator substrate.

The PSi substrates are considered to be a flexible material because of the presence of a large number of pores and a coherent assembly of small crystalline columns with dimensions varying from 30 to 300 Å^[5]. Thus, the stress due to the large lattice mismatch and thermal expansion coefficient is relaxed by straining small crystalline columns in PSi layer, instead of the formation of misfit dislocation.

Hasegawa et al ^[5] has studied the growth of GaAs layer directly on PSi substrate. However, it remains a

problem that surface morphology is poor ^[6]. The main idea was proposed by Hayashi et al which is to introduce thin Si epilayer on PSi layer to improve the surface morphology^[7]. GaAs films has been grown on Si/PSi/Si substrate by chemical beam epitaxy in anticipation that the total defect density of the films would be reduced by low growth temperature as compared to metalorganic chemical vapour deposition^[6]. It has been found that the twodimensional (2D) growth, compared to the threedimensional growth (3D), forms a reducer's dislocation density. Kitahara et al have shown that the use of atomic layer epitaxy (ALE) at the initial stages of GaAs growth on Si, produces a two-dimensional growth^[8]. We have used this result to growth a thin GaAs layer where the initial pre-deposition stage is performed by (ALE) using a metalorganic chemical vapour deposition (MOCVD) system.

In this paper, we report the growth of GaAs epilayers on PSi using two-step growth procedure. The initial low-temperature growth of a GaAs thin nucleation layer is done by ALE on PSi to improve the morphology and reduce the dislocation density in GaAs layer. In order to analyse the quality of the GaAs layers, we have used grazing DRX, AFM image and photoluminescence (PL) techniques.

EXPERIMENTAL PROCEDURE

The porous silicon (10 um) layer were formed by anodisation of the Si substrate in 40% HF: C_2H_5OH (1:1). The substrate used were (100) oriented, boron-doped p-type silicon with (1-2 Ω cm) resistively. The

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etch current density was 10 mA cm⁻². The GaAs layers were grown in an EMCORE D125 MOVPE system at a working pressure of 60 Torr. Trimethylgallium and arsine were used as precursors. The growth temperature was fixed at 550°C for the ALE of the GaAs layer. During the ALE step, Ga and As precursors are provided literately^[9], whereas for conventional GaAs growth sequences, Ga and As precursors are provided at the same time. The samples were cleaned in a low concentration HF solution and rinsed with deionised water. The growth of sample was preceded by an annealing step at 700°C under arsine flux in order to remove the native oxide and to passivity the surface by arsenic atoms. Then the growth temperature was ramped down to 550°C. The set of samples with lowtemperature process is consisted to growth of GaAs layer on PSi substrate and on silicon substrate, are noted respectely LTGaAS-PSi and LTGaAs-Si. The stage of process will start by grown a 124 Å thin GaAs layer directly grown on PSi and on silicon substrates at 550 °C using ALE technique, followed by a 1000 Å thick layer of GaAs without using the ALE technique. A set of samples at high-temperature growth, consists in a 124 Å thin film of GaAs at 550°C using ALE technique on porous silicon and on silicon substrates followed by 1200 Å GaAs layer without the ALE technique, the temperature was ramped to 700°C, these layers are denoted respectively HTGaAs-PSi and HTGaAs-Si.

The photoluminescence measurements were performed using a variable temperature (10 K - 300 K) close-cycle cryostat under 514.5 nm line of an Argon ion Ar+ laser as excitation source. The signal was detected through a 250 mm Jobin-Yvon monochromator and by GaAs photomultiplier. The AFM micrographic of GaAs film was measured using nanoscope 3 of Digital Instrument (Veeco). The DRX curve was recorded by PANalytical Diffractometer.

RESULTS AND DISCUSSION

In order to determine and verify the phase formation of GaAs on porous silicon, XRD analyses were carried out in the 10° - 70° range of 2Θ . The Fig. 1 shows the XRD grazing spectra of LTGaAs-PSi and HTGaAs-PSi substrates. This pattern confirm the formation of GaAs phase with a large broader peak centred near 53.74° and other relative diffusion peak at 2Θ on 27.25°, 45.34° and 72.93°. The position and the relative intensity are identifying from the ICSD file. The position of these peaks closely resembles of cubic (F-43m) structure with ref 01-080-0016. In Fig. 1a, it can be seen an other peak at 54,71° that it is attributed to AsSi monoclinic phase with reference 03-065-1235. In addition, there is other reflection are found in Fig. 1(b) that it's attributed to gallium oxide phase

The GaAs nucleation layer morphology depends of the growth condition as shown by AFM measurements. Figs. 2 (a) and 2 (b) show AFM images of the sample grown with LT process respectively on PSi and on Si substrates. The AFM images reveal the formation of GaAs grains which tend to be arranged parallel to the^[11] azimuth. The surface morphology is formed by agglomeration of small grains. Figs. 2 (c) and 2 (d) show the result of the sample grown with HT process on respectively PSi and silicon substrate. The grain size uniformity is slightly imperfect in all samples and the grains alignment worsens as the grain size increases. We suggest that the increase in the grain size is due to the HT process of the GaAs nucleation stage and the uniform distribution and alignment of grains is due to the LT process We notice that with the LT process there is an agglomeration of a small grain size which is attributed to the coalescence mechanism which may not be finished. For the HT process, it' the coalescence is due to the big grain size.



Fig.1: XRD grazing spectra of resultant: (a) LTGaAs-PSi (b) HTGaAs-PSi



Fig.2: AFM micrographs of (a) LTGaAs-PSi , (b) LTGaAs-Si, (c) HTGaAs-PSi and (d) HTGaAs-Si.

Fig. 3 shows the PL spectrum as function of temperature under 60mW laser power excitation. The PL spectra exhibit an asymmetrical curve. The spectra are fitted by two Gaussian curves: P1 at 1,41 eV and P2 at 1,49 eV distant of about 80 meV for LTGaAs-PSi and P1 at 1,42 eV and P2 at 1,49 eV distant of about 70 meV for HTGaAs-PSi. The Fig. 4 shows the peak position of HTGaAs-PSi and BTGaAs-PSi as function of temperature in the range of 10 to 300K under 60 mW as laser power excitation. As showing in Figs. 4 (a) and (b), the energy of P_1 transition remain constant at 1.42 eV, this effect result in fact that the P₁ peak is originate impurity transition as a carbon defect-acceptor of recombination process[10]. However, the P₂ peak position decreases with increase temperature. The P₂ transition corresponds to а band-to-acceptor recombination.



Fig. 3: PL spectrum for (a) LTGaAs-PSi, (b) HTGaAs-PSi

Fig 5 (a) and (b) show respectively the 8 K photoluminescence spectra of sample LTGaAs-PSi compared to LTGaAs-Si and HTGaAS-PSi compared to HTGaAs-Si. The PL spectrum of the Si-doped GaAs substrate consists of an emission line at 1.485 eV. This transition is attributed to the conduction band-to-neutral Si acceptor [11]. The red-shift observed, compared to GaAs intrinsic band gap at 1.51eV, is due to the large number of gallium vacancies and anti-site defects that can be filled by the small Si atoms. The equation (1) gives the values of the hole concentration p calculated from the shift of PL according to the empirical band-gap shrinkage formula^[12]

$$\Delta E_{\rm G} = -2.6 \times 10^{-8} \, {\rm p}^{1/3} \tag{1}$$

where the hole concentration p is in cm⁻³ and the energy-gap shrinkage ΔE_G in eV.

In our case the values of the free hole density p calculated from PL data are $4.42 \ 10^{18} \text{ cm}^{-3}$ for HTGaAs-PSi and $6.05 \ 10^{17} \text{ cm}^{-3}$ for LTGaAs-PSi.

The results of Tabata ^[13] and Bensaada ^[14] show that the PL analyses can be used to measure strain. The half–width of the PL peak increases with the misfit dislocations. Fig. 5(a) shows that the PL half-width of LTGaAs-Si is larger than of LTGaAs-PSi sample. On the other hand, PL half-width of HTGaAs-Si is lower than of HTGaAs-PSi, Fig. 5(b).



Fig. 4: Peak position versus temperature (a) BTGaAs-PSi (b) HTGaAs-Si

This result affirms that in LT process the strain density in GaAs layer decreases using PSi as substrate. On the other hand in HT process, the strain density decreases by using Si as substrate. The increase of the train density in GaAs on PSi substrate while passing from LT to HT processes may be explain by the thermal strain introduced during cooling. The strain is easily absorbed by the porous region at low temperature; on the other hand at high temperature the porous region may be relaxed.

In addition, we note in Fig. 5 (b), a significant redshift in HTGaAs-PSi PL spectra compared to HTGaAs-Si. This effect confirm that HT process increase the stress induced by the thermal expansion coefficient between GaAs and the residual Si(~ 70 %). At high thermal process the PSi skeleton can be breaks and then the structure can be relaxed. These results are correlated to analysis by AFM measurements. The AFM images show that the HTGaAs on P Si is formed by low grain density with big grain size compared to HTGaAs on Si substrate. This observation indicates that the HTGaAs on P Si is relaxed. The energy induced by the formation of dislocations acts as a non radiative centre to decrease the optical proprieties of GaAs film.



Fig. 5: Photoluminescence spectra at 8K (a) compared spectra for LTGaAs-PSi and LTGaAs-Si (b) compared spectra for HTGaAs-PSi and HTGaAs-Si

In addition, we note in Figs 5, that the PL spectra of LTGaAs-P Si is six times more intense than LTGaAs- Si sample and the PL spectra of HTGaAs-Si is twice more intense than of HTGaAs-P Si sample. On the other hand, the PL spectrum of LTGaAs-P Si is three times more intense than of HTGaAs-P Si sample. The increase of photoluminescence intensity is correlated to the decrease of the tress density and then to the density of electron traps.

CONCLUSION

GaAs epilayer has been grown on Si substrate with an intermediate porous region using the ALE technique. The morphology and PL intensity are improved using a low temperature growth. The high growth temperature increases the grain size and the strain on porous silicon. The LTGaAs- Si using ALE process is promising technique for the development of optoelectronic hybrid devices.

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