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A Fully Integrated Dual-Band Low Noise Amplifier for IEEE 802.11 and Hiper LAN Application

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Abstract: A fully-integrated dual-band Low Noise Amplifier (LNA), which can be used for IEEE 802.11 and Hiper LAN applications, was investigated in this paper. The proposed LAN was implemented entirely pm a single chip based on a standard 0.18 μm 1P6M CMOS process. It draws 13 mA current from a 1.5-V voltage supply and achieves power gains of 17 and 10 dB, noise figure of 3.7 and 4.2 dB at 2.4 and 5.3 GHz respectively.

Key word: Low Noise Amplifier (LNA), Dual Band, IEEE 802.11 and HiperLAN

INTRODUCTION

COMS technology is becoming to a suitable technology for implementing wireless portable communication for terminals due to the fact that the gate lengths of MOS devices have been scaled down to submicron regime. Furthermore, by incorporating its high integration level and low cost, COMS technology is a good candidate for RF/analogue/digital mixed signal application. At percent, there exist many communication standards due to the rapid growth of wireless service industry (e.g., Fig. 1). Therefore, a multi-standard COMS RF single chip solution for wireless communication system is expected to be realized. In practice, one of the key bottlenecks for developing a single-chip multi-functional communication device is to design a fully-integrated dual-band/multi-band Low Noise Amplifier (LNA) owing to the LAN's importance in the receiving path of current wireless communication systems. For this purpose, a fully integrated dual-band LAN which is able to provide simultaneous gains at two different frequency bands (2.4GHz-2.5GHz and 5.15GHz-5.35GHz), based on Chartered Semiconductor Manufacturing (CSM) 0.18μm CMOS technology, will be invested in this paper.

Dual-band LAN designs:

Input stage matching: LAN designers usually pay much attention to the input matching design, because the matching quality will greatly influence the overall performance of the designed LAN. Recent research shows that the optimal input stage topology, which has a small Noise Figure (NF) and a reasonable gain, is the source inductive degeneration input stage[1], as shown in Fig. 2(a). Its input impedance can be expressed as:

$$Z_{in} = \{\left[\frac{g_{m1}}{C_{gs}}\right] L_s\} + \{j\omega L_s + j\omega L_s + \frac{1}{j\omega C_{gs}}\} \qquad (1)$$

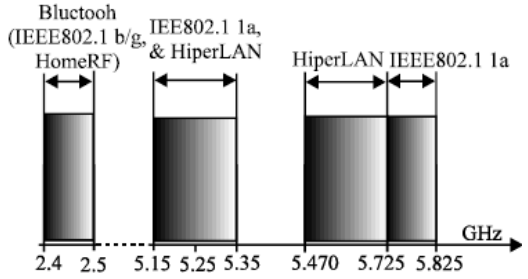


Fig. 1: Communication standard distribution in the range of 2.4-6GHz

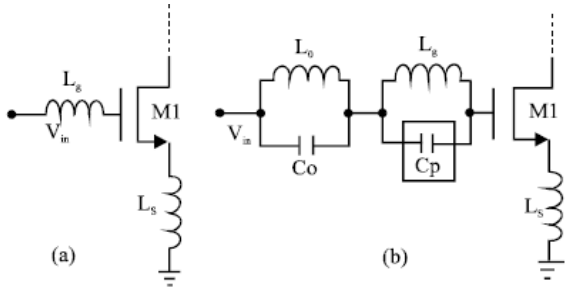


Fig. 2: Source inductive degeneration input stage (b) Modified dual-band input stage

To get a 50Ω, whereas the imaginary part should be zero at the frequency of interest ($\omega_{0=}1/\sqrt{(L_g + L_s)C_{gs}}$). This is the design rule for single-band LAN, similar topology can be adopted. However, one must introduce another zero point (corresponding to ω_{02}) to the imaginary part, since the dual-band LAN has to operate in two different frequency bands (2.4GHz-2.5GHz and 5.15GHz-5.35GHz in this design). The zero point can be achieved by connecting an additional parallel L_0C_0 network in series with the gate inductor L_g[2,3]. The corresponding input impedance is:

$$Z_{in} = \{j\omega L_s + j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\} + \{g_{m1} L_s / C_{gs}\} \quad (2)$$

Unfortunately, in order to realize the series resonance with M1's gate to source capacitance C_{gs} (about 0.23pF for a 240μm/0.18μm NMOS transistor) at a certain frequency, L_g has to be very large. Sometimes it is up to 10 nH[3]. It is known a large and high quality factor (Q) inductor is difficult to be implemented on chip with a standard CMOS process. Even if it was implemented, it consumes a large area (e.g., a radius of more than 125μm with CSM 0.18μm CMOS technology). Moreover, to ensure the normal operation of the on-chip inductor, the distance between the inductor and any other components should be at least 50 μm when drawing layout[4]. It means a 10nH inductor will occupy an area with a radius of at least 175 μm, which is very costly. Therefore, to reduce the cost, come modification is done with our work. A capacitor C_p is connected in parallel with L_g, as depicted in Fig. 2(b). To this topology, input impendence can be derived as:

$$Z_{in} = \{j\omega L_s + \frac{j\omega L_{g2}}{1-\omega^2 L_{g2} C_p} + \frac{1}{j\omega C_{gs}} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\} + \{g_{m1} L_s / C_{gs}\} \quad (3)$$

In contrast with (2), the effect of C_p (about 1_pF, which occupies 30μm×30μm area), L_g can be reduced to 2nd (65μm radius). Consequently, up to 56% chip area is saved, as summarized in Table 1. Fig. 3 compares the input reflection coefficients S_{11_1} and S_{11_2} under the conditions without C_p (L_g = 10nH, C_p = 0) and with C_p (L_g = 2nd, C_p = 1pF). The pot indicates S_{11_2} does not degrade at the required frequency bands and proves the availability of the above mentioned area-reducing method.

Noise figure optimization:

Noise sources: a small NF is another common consideration in LNA designs, in a MOS device, the dominant noise sources are drain channel noise $\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f$ and gate induced noise $\overline{i_{n,d}^2} = 4kT\delta g_g \Delta f$ [5-8]. Other prominent noise sources are gate parasitic resistance thermal noise i_{n,R_G}^2 substrate thermal noise $i_{n,Sub}^2$ and $i_{n,corr}^2$, which is due to the correlation of $i_{n,g}^2$ and $i_{n,d}^2$. Fig. 4 gives a visual illustration and Fig. 5 depicts an equivalent circuit with noise sources of the proposed dual-band LNA.

Table 1: Comparison of L_{g1} and L_{g2}

	L_{g1} (without Cp)	L_{g2} (C_p connected)
Inductance (nH)	10	2
Radius including the	50	
μm outside the inductor	175μm	115μm
Area (mm^2)	0.0962	0.0415
Area of C^p (mm^2)	0	0.0009
Sum (mm^2)	0.0962	0.0424
Saved area (%)	0	56

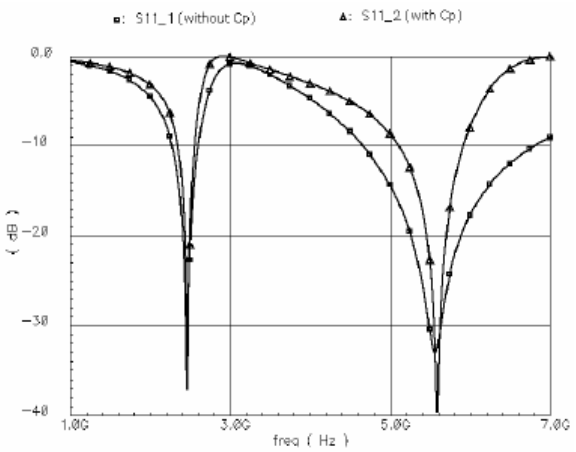


Fig. 3: Comparison of S_{11} @ L_{g1} = 10nH, C_p =0 and L_{g2} =2nH, C_p =1pH

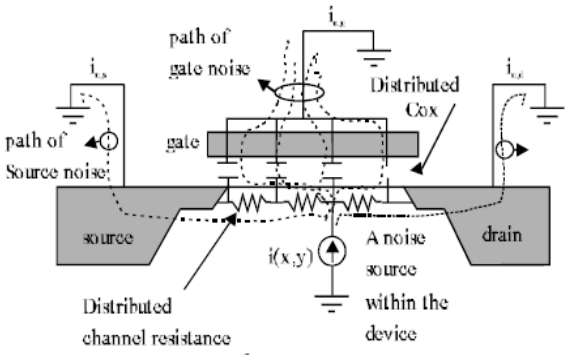


Fig. 4: Description of various noise sources in a MOS transistor[5]

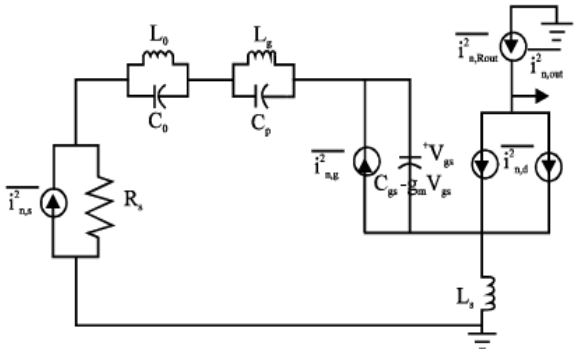


Fig. 5: Small signal equivalent circuit with noise sources of the proposed dual-band LNA

Output noise: According to Fig. 5, through circuit analysis, the transfer function of the various noise sources can be achieved. Then the corresponding output noise is expressed as follows:

$$\overline{i^2_{n,0,Rs}} = \left|\frac{g_m R_s}{j2\omega_0 C_{gs} R_s + j\omega C_{gsD_0}}\right|^2 \overline{i^2}_{n,Rs} \tag{4}$$

$$\overline{i^2_{n,o,d}} = \frac{1}{4}\overline{i^2_{n,d}} \tag{5}$$

$$\overline{i^2_{n,o,g}} = \left|\frac{\frac{g_m}{j2\omega_0 C_{gs}}}{(1-\frac{1}{j\omega_0 C_{gs} R_s + j\omega C_{gs} D_0})}\right|^2 \overline{i^2_{n,g}} \tag{6}$$

$$\overline{i^2_{n,o,R_{out}}} = \overline{i^2_{n,R_{out}}} \tag{7}$$

$$\overline{i^2_{n,o,corr}} = \frac{g_m |c|}{2\omega_0 C_{gs}} (1-\frac{j\omega C_{gs} D_0}{(j\omega C_{gs})^2 D_0^2 + \omega^2 C_{gs}^2 R_s^2})\sqrt{\overline{i^2_{n,g}}.\overline{i^2_{n,d}}} \tag{8}$$

Is the imaginary part of the input impedance (see (3)) and equal to zero at the two corresponding resonant frequencies (2.45GHz and 5.3GHz in this paper). In terms of the above equations, the noise factor noise can be obtained:

$$\begin{aligned} F &= \frac{\overline{i^2_{n,0,Rs}} + \overline{i^2_{n,0,g}} + \overline{i^2_{n,0,d}} + \overline{i^2_{n,0,corr}} + \overline{i^2_{n,0,R_{out}}}}{} \\ &= 1 + \frac{\delta\alpha}{5 g_m R_s}\{(j\omega C_{gs} D_0 - 1)^2 + \omega^2 C_{gs}^2 R_s{}^2\} \\ &+ \frac{\gamma}{\alpha g_m R_s}\{(j\omega C_{gs} D_0)^2 + \omega^2 C_{gs}^2 R_s{}^2\} + \frac{2|c|}{g_m R_s} \\ &\sqrt{\frac{\gamma\delta}{5}}\{(j\omega C_{gs} D_0 + \omega^2 C_{gs}^2 R_s{}^2\} \end{aligned} \tag{9}$$

The noise factor at resonance frequency ω_0 ($D_0 = 0$ under this condition) can be achieved as well:

$$\begin{aligned} F_0 &= 1 + \frac{\delta\alpha}{5 g_m R_s}\{1 + \omega_0^2 C_{gs}^2 R_s{}^2\}\frac{\gamma}{\alpha g_m R_s} \\ &+ \omega_0^2 C_{gs}^2 R_s{}^2 + \frac{2|c|}{g_m R_s}\sqrt{\frac{\gamma\delta}{5}}\omega_0^2 C_{gs}^2 R_s{}^2 \end{aligned} \tag{10}$$

Noise optimization: In CMOS LNAs the MOS transistor usually operates in saturation region[6], a simplified equation for the drain current I_{ds} when the transistor operates in saturation is[7]:

$$I_{ds} = \frac{W}{2\xi L_{eff}}\mu_{eff} C_{o\chi}(V_{GS} - V_T)^2 \tag{11}$$

where, μ_{eff} is the carrier effective mobility in the transistor channel and ξ is a factor, which takes the short channel effect and other effect into account and is often set to one in the simplified MOS transistor model, but can be significantly larger in short channel MOS transistors. Taking the derivative of (11) with respect to V_{GS} yields:

$$g_m = \frac{W}{\xi L_{eff}}\mu_{eff} C_{o\chi}(V_{GS} - V_T) = \sqrt{\frac{2W}{\xi L_{eff}}}\mu_{eff} C_{o\chi} I_{ds} \tag{12}$$

Combining (9), (12), $C_{gs} \approx \frac{2}{3} WLC_{o\chi}$ [7, 8] and other parameters, the relationship of NF versus frequency can be plotted, shown in Fig. 6.

In practice, we are more interested in the NF at the resonant frequencies such as 2.45GHz and 5.3GHz. According to the expressions of g^m and C_{gs}, (10) can be rewritten as:

$$F_0 = 1 + \frac{R_G}{R_s} + b_1 W^{-1/2} + b_2 \omega_0^2 L_{eff}^2 W^{3/2} \tag{13}$$

where, b_1 and b_2 are equation coefficients. In terms of (13), group of plots is presented. Fig. 7 gives a plot of NF versus transistor width (W) at frequencies 2.45GHz and 5.3GHz respectively; Fig. 8(a) and (b) depicts the relationship among NF, W and the drain current I_{ds}, which is corresponding to the LAN's power consumption $P_d = V_{dd} I_{ds}$. It can be found that (13) contains terms which are constant, proportional to W. Therefore, there must corresponding to the minimum noise factor. Different (13) with respect to W and equate it to zero yields.

$$W_{opt} = \sqrt{\frac{b_1}{3 b_2 \omega_0^2 L_{eff}^2}} \tag{14}$$

For a fixed current I_{ds} = 8mA, (14) generates two W_{opt} values of W_{opt1} = 240μm and W_{opt2} = 110 μm corresponding to f_{01} = 2.45 GHz and f_{01} 5.3 GHz respectively. Hence a tradeoff between W_{opt1} and W_{opt2} has to be made. A transistor width of 200 μm is finally chosen after consideration of various factors, such as the gain and NF as well as the circuit stability. Fig.9 compares the NF with different W of 240 μm, 110 μm and 200 μm. Following the above procedure and plots, one can optimize the LNA according to different design requirements.

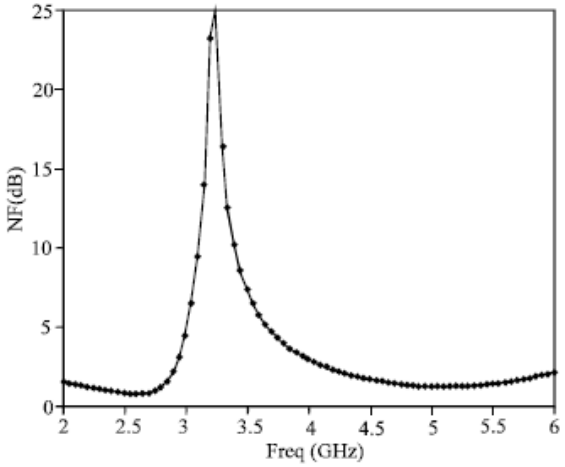


Fig. 6: NF vs. Freq, for W/L =240μm/0.18μm, γ =1.8, δ =3, ξ=1.6, α =0.8, μ_{eff} = 0.035m^2/V,

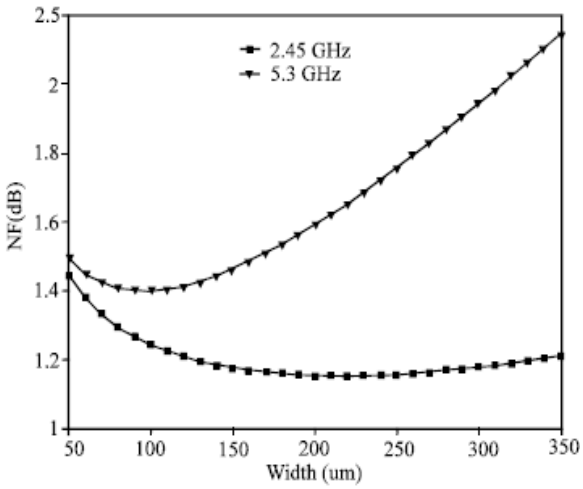
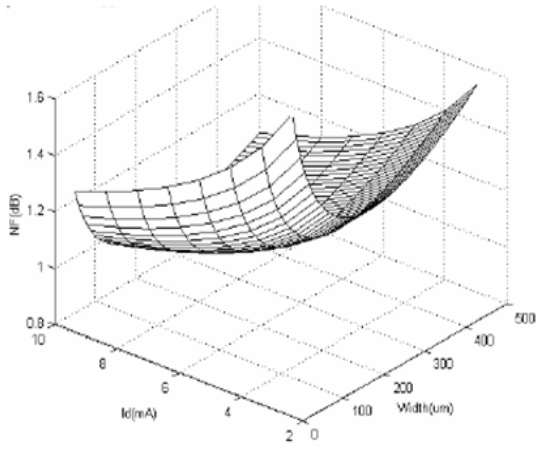
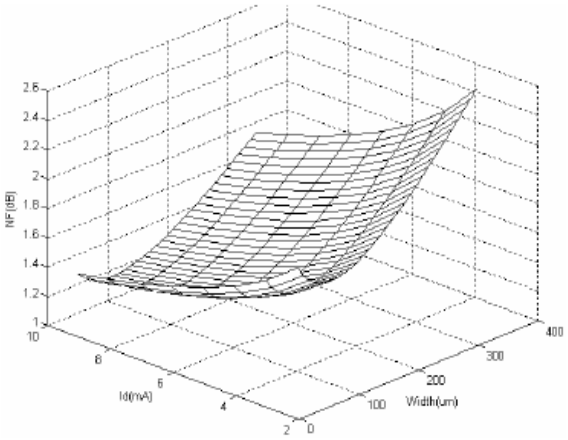


Fig. 7: NF vs. W forγ =1.8, δ =3, ξ=1. 6, α =0. 8, μ_{eff} =0. 035m^2/V, C_{ox} 0. 008F/m^2 and I_{ds} = 8mA



(a)



(b)

Fig. 8: NF vs. W and I_{ds} for (a) f_{01} = 2.45GHz and (b) f_{02} =5. 3GHz

LNA implementation and measurement results: Based on the above analysis, a concurrent dual-band LNA is designed. Figure 10 is the simplified schematic diagram. It is a two-stage amplifier with an additional buffer stage for output matching purposes. In the LNA, cascade structure is used to reduce the influence of the influence of the gate-to-drain overlap capacitance V_{gd} on LNA's input impendence and to improve the LNA's reverse isolation to prevent the Local Oscillator (LO) feed through from the subsequent mixer back to the LNA's RF input. In the circuit, the dimension of the M2 is the same as M1; whereas M3 and M4 have the same dimension of 150μm/0.18μm. The selection of L_1 and L_2 is based on the resonant frequency and quality factor for a certain power gain. Capacitor C_e is a Q-enhancement capacitor[9].

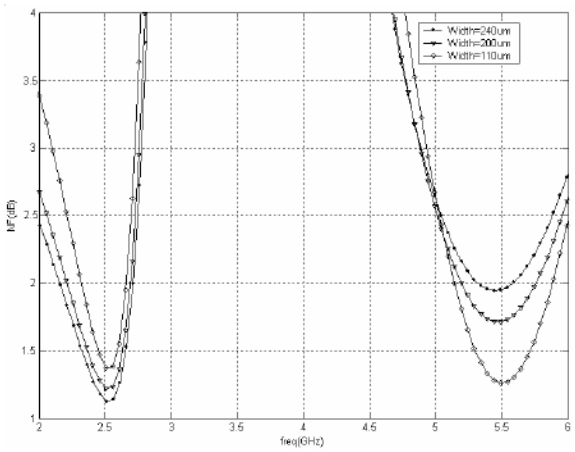


Fig. 9: NF with different transistor widths

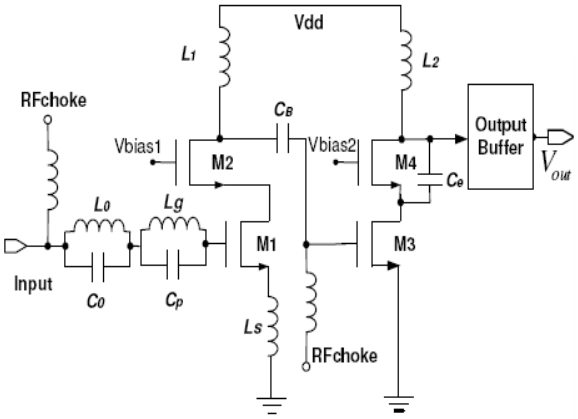


Fig. 10: Simplified schematic diagram of the dual-band LNA

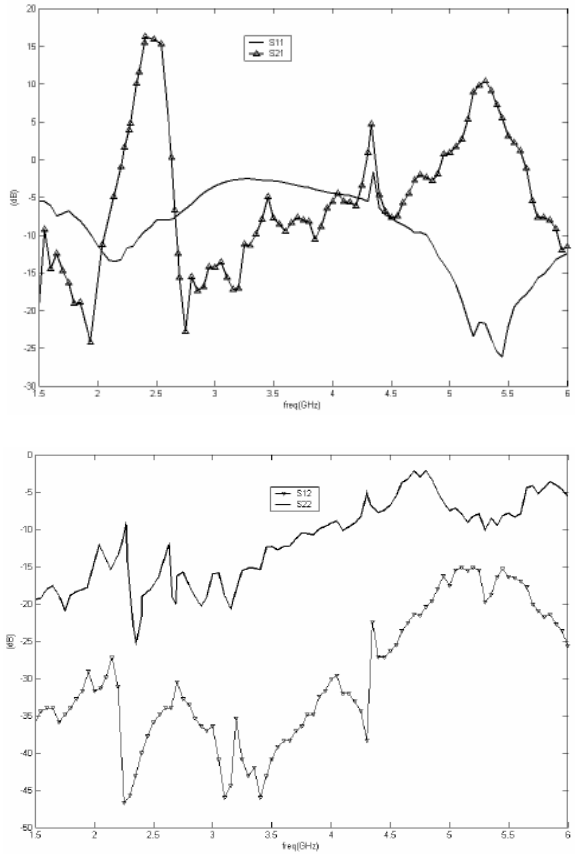


Fig. 11: Measured S-parameters of the dual-band LNA

Table 2: detailed performance of the dual-band LNA

	1st band	2nd band
V_{dd} (V)	1.5	
P_d (mW)	21	
Operating band (GHz)	2.4-2.5	5.15-5.4
S_{11} (dB)	-12 - -8	-25 - -20
S_{22} (dB)	-20 - -18	-8 - -7
S_{12} (dB)	-35 -	-16
NF (dB)	3.7	4.2

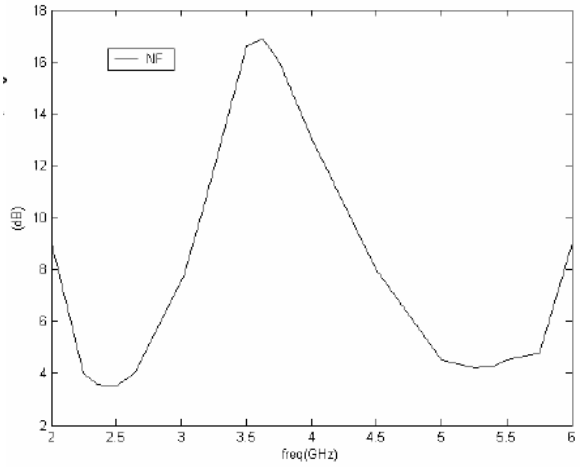


Fig. 12: Measured noise figure

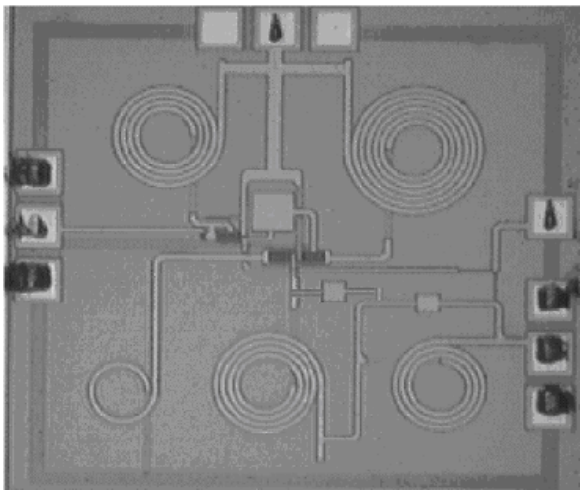


Fig. 13: Die photo of the dual-band LNA (0.8mm×0.85mm)

Properly adjusting the parameters of the passive and active components of the schematic can make the LNA work at two different frequency bands at the same time, which is meaningful for the development of multi-standard operation devices. The proposed dual-band LNA was fabricated at CSM and was measured using a HP8510C network analyzer with on-wafer RF probes. Fig. 11 and 12 demonstrate the measured S-parameters and noise figure. It is shown that the LNA has a power gain of about 17dB at the first band and a gain of 8-10dB at the second band. Detailed performance can be found in Table 2. Fig. 13 is the die photo of the proposed dual-band LNA.

DISCUSSION

The parasitic resistance of the on-chip inductors: The measurement data indicate that the LNA's noise figure is not as good as GaAs devised.

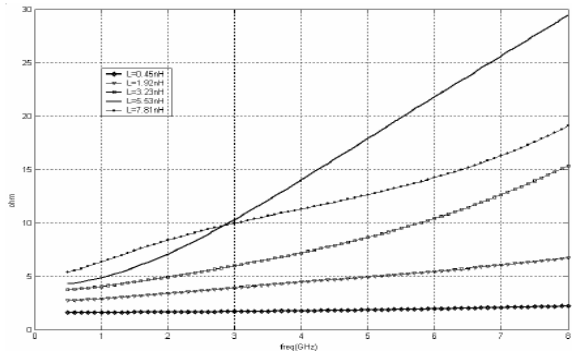


Fig. 14: Parasitic resistance of several on-chip inductors based on a standard CMOS process

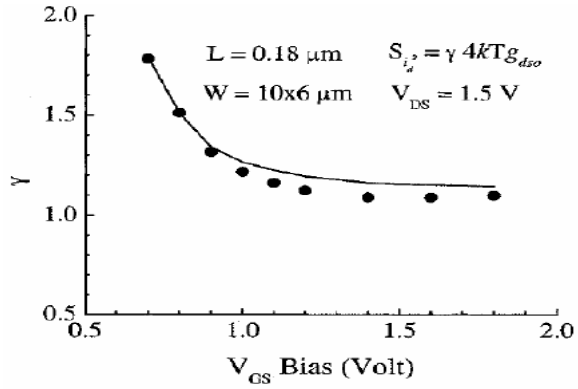


Fig. 15: γ versus V_{GS} characteristics of n MOSFET[10]

This is mainly due to the loss on-chip integrated inductors in a standard CMOS technology. In practice, the parasitic resistance of the low-Q inductors has a severe impact on the LNA's noise performance. Figure 14 presents the parasitic resistance R_p versus frequency of several on-chip inductors based on CSM 0.18 μm CMOS process. The figure shows that R_p increases with frequency. For a 1.92nH inductor, its R_p is about 5Ω at 5.3GHz; whereas for a 7.81nH inductor, the 50Ω single source resistance R_s. Therefore, when designing and LNA, one should avoid using large inductance inductors, since their RP is relative larger compared to the smaller ones. Additionally, the parasitic resistance of the on-chip inductors must be taken into account when doing noise optimization for a more accurate noise figure prediction. Generally, the total R_p of all the on-chip inductors of an LNA's overall figure degradation, R_p can reduce the LNS's gain as well.

Channel noise coefficientγ: channel noise coefficient γ is a bias-dependant factor, for long channel devices, it is between 1 (in the linear region with V_{ds} = 0) and 2/3 in saturation[8]. For short channel devices γ is much greater due to short channel effects such as channel-length modulation and velocity saturation. There does not exist a constant value for γ for short channel devices. In the past few years, the value between 1-6 has been used. In terms of Fig. 15.

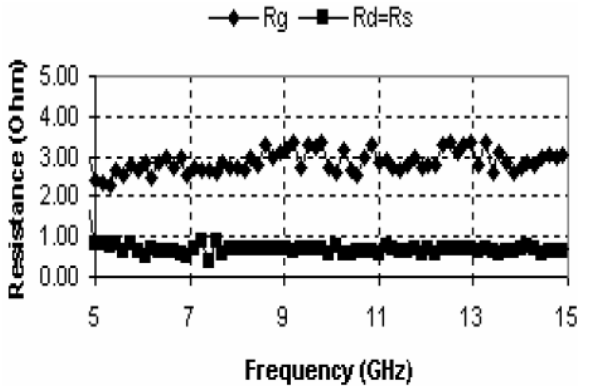


Fig. 16: Terminal resistance of nMOS with L = 0.8μm, W = 8μm and n_f = 25

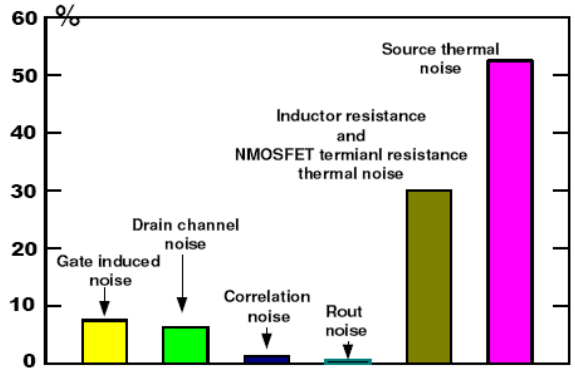


Fig. 17: Noise contribution of different noise sources in a CMOS LNA

Terminal resistance of MOSFET: the gate resistance R_g, source resistance R_s and drain resistance R_d can contribute thermal noise to the total circuit as well. Fig. 16 illustrates the terminal resistance versus frequency for a transistor size of 200μm/0.18μm. It can be found that the total terminal resistance of the n MOSFET is about 5Ω, which provides about 5% noise contribution.

We finally summarize the noise contribution of the various noise sources in a fully-integrated CMOS LNA as shown in Fig. 17. The statistic figure indicates the obstacle for RF circuit designs. How to achieve high-Q, low cost on-chip passive components are an urgent problem to be solved.

CONCLUSION

A CMOS dual-band low noise amplifier has been investigated in this paper. The LNA has two investigated in this paper. The LNA has two pass bands and can be used for Bluetooth, wireless LNA and Hiper LNA applications. The LNA is implemented entirely on a single-chip and is possible to be integrated with other CMOS devices. In this paper, a method to reduce the gate inductor as well as a procedure for dual-band LNA

noise optimization is also presented. The design of the proposed LNA indicates with the ever-continuing downscaling of CMOS technologies, a fully-integrated multi-standard operation wireless communication system implemented using a low cost CMOS process becomes possible.

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